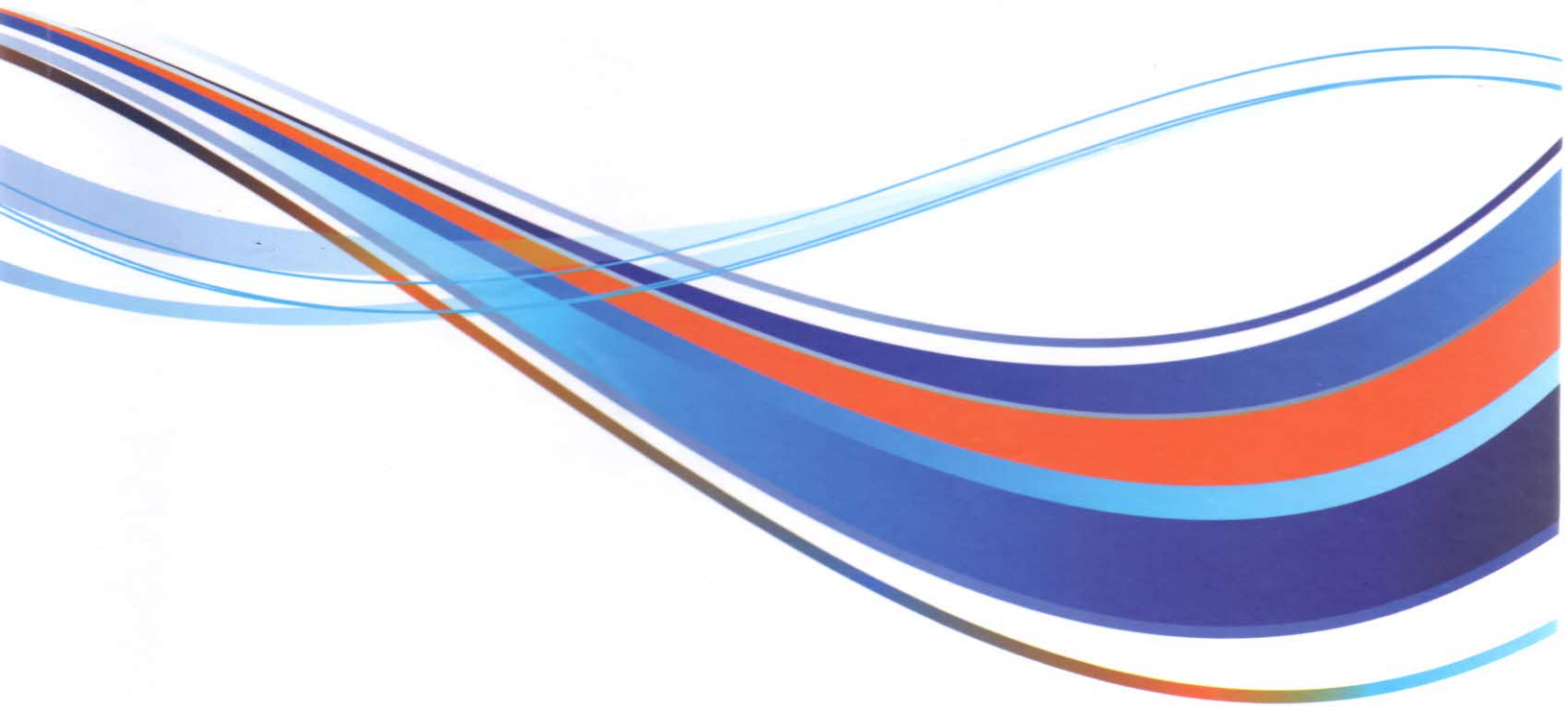
In-house Qualified Processes for Hi-Rel Electronic & Microelectronic Fabrication, Assembly & Surface Treatment



Space Applications Centre, ISRO
Ahmedabad

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MESSAGE

Space Applications Centre (SAC) is responsible for design and development of Satellite Communication (SATCOM), Navigation, Remote Sensing, Space Science and planetary exploration payloads using state-of-the-art technologies for the miniaturization, weight reduction, and reliable operations. Presently SAC is carrying out design, fabrication, assembly, testing and evaluation activities up to 60 GHz for Inter Satellite Link (ISL) and Temperature Sounding Unit (TSU). In future these capabilities are to be extended up to 220 GHz for Humidity Sounding Unit (HSU) etc.

In order to manufacture these state-of-the-art complex payloads, SAC have to qualify each and every process before using them for actual hardware

This document provides details of ***in-house qualified processes*** related to Hi-Rel electronic and microelectronic fabrication and assembly and surface treatment along with major specifications. I hope, this document would be very much useful to SAC/ISRO industrial partners to identify the processes of their interest for know-how transfer. SAC will be very happy to share the technology to Indian industry to take a step forward towards *"Make in India Programme"*.

Tapan Misra

Place: Ahmedabad
Date: 1 February 2016

(तपन मिश्रा)
(Tapan Misra)

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Message

An excellent document is made by Electronic Support Services Area (ESSA) team by compiling the in-house developed, qualified processes for *Hi-Rel electronic and microelectronic fabrication & assembly and surface treatment*. It also covers the salient features along with major specifications of respective qualified process.

This document will not only be useful for Space Applications Centre (SAC), ISRO community, but will be potential source for our industrial partners to identify the qualified process for manufacturing of space hardware and subsequently to acquire the knowhow from Technology Transfer & Industrial Interface Division (TTID).

राजकुमार अरोड़ा

Ahmedabad
1st February 2016

(राजकुमार अरोड़ा)
Rajkumar Arora

Document Control Sheet

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2	**Title & Sub Title**	Summary on in-house qualified processes for Hi-Rel Electronic and Microelectronic Fabrication, Assembly and Surface Treatment as on February 2016.
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8	**Approved by**	DD, ESSA
9	**Abstract**	This document details out the Qualified Process for Fabrication of Micro electronics, SAW, PCBs fabrication, wiring and assembly, Surface Treatment & Thermal Control Coating for Space use.
10	**Security Classification**	Unclassified

Table of Contents

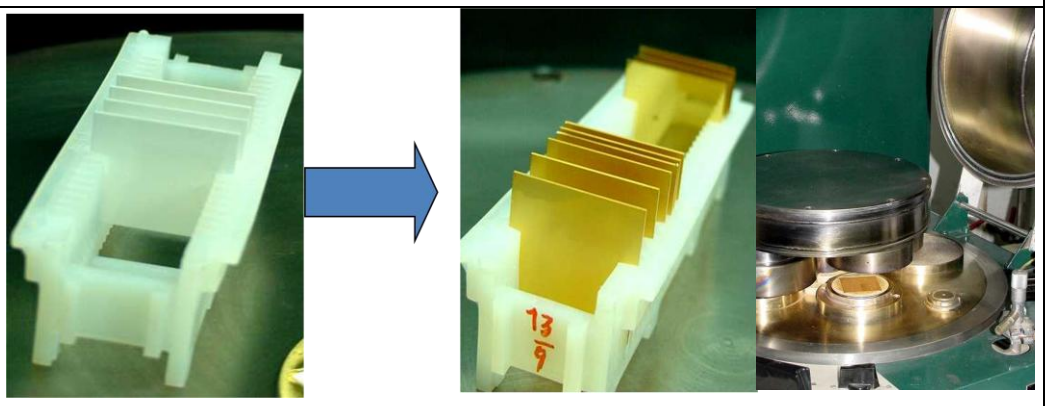
Introduction

Space Applications Centre, Indian Space Research Organisation (ISRO) is responsible for design and development of various State of the art SATCOM, Navigation, Microwave and Optical remote sensing payloads for various societal and national applications. For reliable operation of payload, it has to meet very high reliability of the order of zero defects. In order to meet the assigned reliability every circuit, subsystem and payload have to undergo various reviews and they have to be fabricated and assembled using various qualified processes.

The respective subsystems and payloads undergo rigorous Test and Evaluation procedure. The qualified processes at Space Applications Centre (SAC) for fabrication and assembly of Microelectronics, SAW devices, PCBs, and Surface treatment on packages are summarized in this document titled as “In-house Qualified Processes for Hi-Rel Electronic and Microelectronic Fabrication, Assembly and Surface Treatment”. This document will be very much useful to Technology Transfer and Industry Interface Division for technology transfer to Indian Industries to meet the enhanced Indian Space Research Organisation (ISRO) projects requirement.

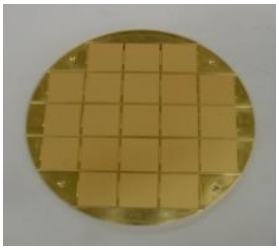
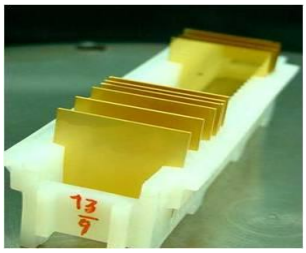
1. Substrates processing (Cutting and Hole Drilling) on 10mil thick bare & metalized Alumina substrates using MS-20 Laser system	
Salient Features	➢ Substrates cutting Hole drilling using MS-20 Laser system ➢ Nd-YAG laser with 1.064 micron wave length ➢ Beam diameter ~150 microns ➢ Power level 0.5 W to 2.0W ➢ Pulse repetition rate 1pulse/sec
Major Specifications of the Qualified Process	➢ 10 mil bare and metallized alumina substrates ➢ Cutting Size 5 mm to 50 mm ➢ Size tolerance ± 100 microns ➢ Hole type circular and square ➢ Hole sizes 1mm to 5mm ➢ Location/positioning accuracy ± 50 microns ➢ Circularity of hole ±50 microns ➢ Edge flatness ±50 microns

2. Cr-Au metallization on 25mil & 10mil thick Alumina substrates using RF Sputtering system	
Salient Features	➢ Cr-Au metallization using Z-400 RF sputtering system ➢ Diode configuration three platform and cathodes of 3” diameter target ➢ 04 Nos. of 1 sq. inch substrates can be accommodate on each platform in single batch ➢ Ultimate vacuum better than 1x10e-6 Bar. ➢ Process Vacuum: 1.0x10e-2 to 4.0x10e-2 Bar. ➢ Argon flow with 2 bar pressure to achieve process vacuum ➢ In situ cleaning by reverse sputtering ➢ Power level: 1.2 kW to 1.6 kW ➢ Plating: Duty cycle: 20% ± 5% ➢ Ontime: 2 ms, Off time: 8 ms ➢ Average Current: 40mA to 60mA (with peak current 0.2A - 0.6A) ➢ Bath temperature: 55 to 65 deg. C ➢ pH value of bath: 4 ± 0.5

Major Specifications of the Qualified Process	➢ Cr ~300 Angstrom ➢ Au 0.5 to 0.7 microns by sputtering and followed by pulse plating to enhance the thickness ➢ Total metal thickness 5.0 to 7 microns. ➢ Uniformity of deposited film ±10% ➢ Sheet Resistivity of metallization: < 0.006 Ω/□
Photograph	

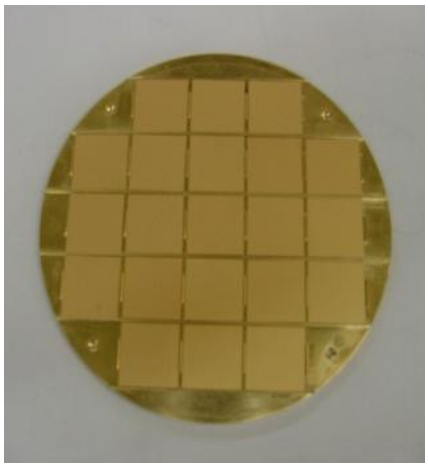
3. Cr-Au metallization on 25mil & 10mil thick Alumina substrates using Magnetron Sputtering system

Salient Features	➢ Cr-Au metallization using Denton Discovery-18 Magnetron sputtering system ➢ Co focal arrangement of three cathodes on 3” target ➢ 21 nos. of 1 sq.in substrates can be accommodate in single batch ➢ Ultimate vacuum better than 1x10e-6 Torr ➢ Process vacuum: 5.0x10e-3 to 2.0x10e-2 Torr ➢ Argon flow: 20 to 35 SCCM ➢ In situ low energy ion cleaning ➢ Rotation speed: ~10 rpm ➢ Power level: 75W to 125W ➢ Plating: Duty cycle: 20% ± 5% ➢ Ontime: 2 ms, Off time: 8 ms ➢ Average Current: 40 to 60mA (with peak current 0.2 A - 0.6A) ➢ Bath temperature: 55 to 65 deg. C ➢ pH value of bath: 4 ± 0.5

Major Specifications of the Qualified Process	➢ Cr ~300 Angstrom ➢ Au 0.5 to 0.7 microns by sputtering and followed by pulse plating to enhance the thickness ➢ Total metal thickness 5.0 to 7 microns. ➢ Uniformity of deposited film ±10% ➢ Sheet Resistivity of metallization: < 0.006 Ω/□
Photograph	   

4. Cr-Cu-Au metallization on 25mil thick Alumina substrates using Magnetron Sputtering system

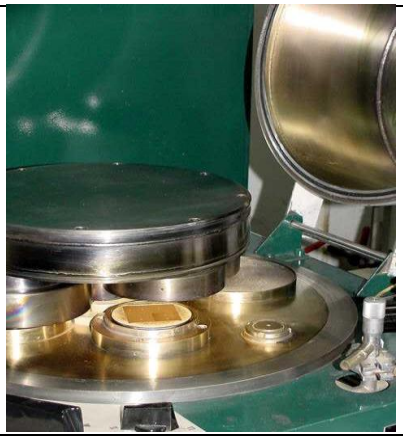
Salient Features	➢ Cr-Cu-Au metallization using Denton Discovery-18 Magnetron sputtering system ➢ Co focal arrangement of three cathodes on 3” target ➢ 21 nos. of 1 sq.in substrates can be accommodate in single batch ➢ Ultimate vacuum better than 1x10e-6 Torr ➢ Process vacuum 5.0x10e-3 to 2.0x10e-2 Torr ➢ Argon flow 20 to 35 SCCM ➢ In situ low energy ion cleaning ➢ Rotation speed ~10 rpm ➢ Power level 75W to 125W

Major Specifications of the Qualified Process	➢ Cr ~300 Angstrom ➢ Cu 4~5 microns ➢ Au 2 microns ±10% ➢ Total metal thickness 5.8 to 7 microns. ➢ Uniformity of deposited film ±10% Sheet Resistivity of the film: <0.006 Ω/□
Photograph	 

5. NiCr/Al metallization on Quartz & LiNbO3	
Salient Features	➢ NiCr/Al metallization over Quartz & LiNbO3 required for Surface Acoustic Wave (SAW) devices, for Space craft Payload applications. ➢ The required metallization was carried out by Vacuum evaporation process employing, NiCr resistively and e-beam gun for Al metallization.
Major Specifications of the Qualified Process	➢ Substrate material: Quartz and LiNbO3 ➢ Substrate size: Piece part of 15mm X 30mm to 4”dia. Wafers ➢ Metallization Thickness range: 1000Å to 2000Å ➢ Thickness Tolerance: ±10% of required metallization thickness ➢ Uniformity of metalized film: ± 3% on 15mm X 30mm substrate size and ± 5% on 4”diameter wafers. ➢ Sheet Resistivity of Al metallization: < 0.6 Ω/□

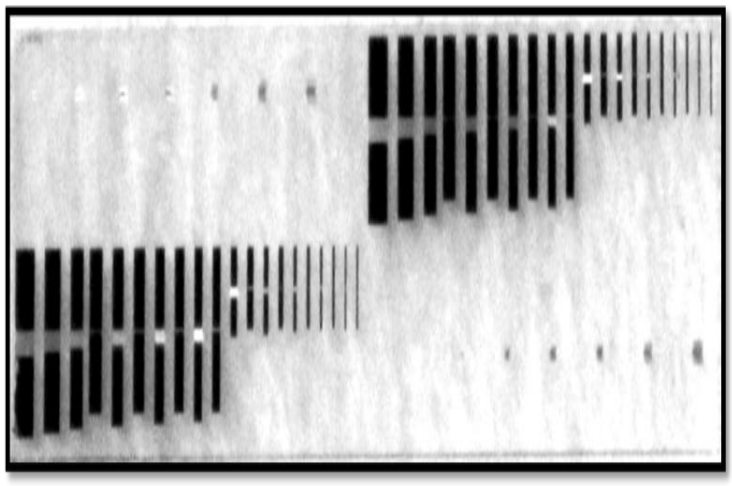
6. Alumina substrate dicing using High Speed Dicing (In-house and Vendors)	
Salient Features	➢ Dicing of metalized and patterned alumina substrate for the various sizes ranging from 2.0X5.0 mm2 to 12.7X25.4 mm2 for Space craft Payload applications. ➢ The required various size was carried out by High speed dicing
Major Specifications of the Qualified Process	➢ Substrate material: Alumina (Metalized and Patterned) ➢ Substrate size: 2.0mmX5.0mm to 12.7mmX25.4mm ➢ Thickness : 25 mil ➢ Metallization : Two layer and Three layer ➢ Edge Flatness: ±35microns ➢ Cutting Accuracy: ± 100 microns

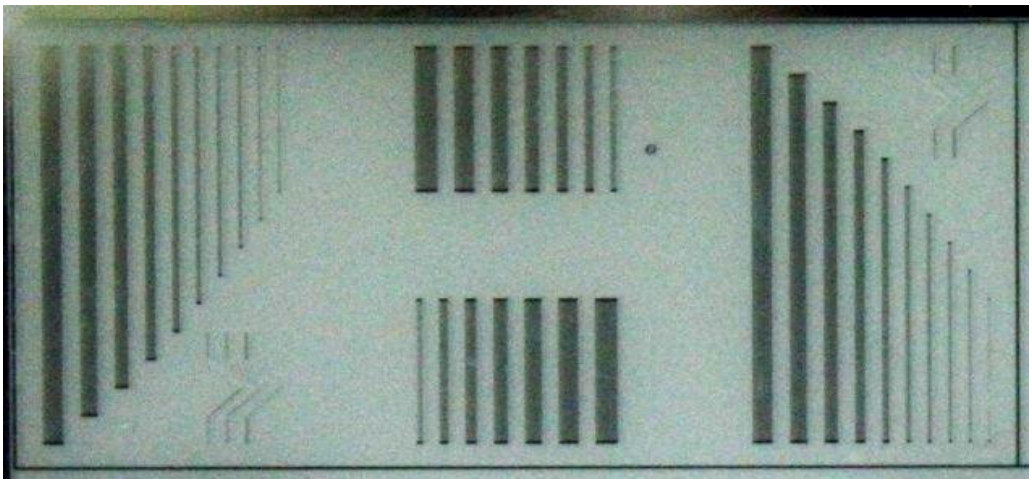
7. Substrates processing (cutting and hole drilling) on 25 mil thick bare & metalized Alumina substrates using MS-20 Laser system	
Salient Features	➢ Substrates cutting Hole drilling using MS-20 Laser system ➢ Nd-YAG laser with 1.064 micron wave length ➢ Beam diameter: ~150 microns ➢ Power level: 0.5 W to 2.0W ➢ Pulse repetition rate: 1pulse/sec
Major Specifications of the Qualified Process	➢ 25 mil bare and metallized alumina substrates ➢ Cutting Size 5 mm to 50 mm ➢ Size tolerance ± 100 microns ➢ Hole type circular and square ➢ Hole sizes: 1mm to 5mm ➢ Location/positioning accuracy: ± 50 microns ➢ Circularity of hole: ±50 microns ➢ Edge flatness: ±50 microns

8. Cr-Au metallization on 10 mil thick Alumina substrates having 500 microns via hole using RF Sputtering System	
Salient Features	➢ Cr-Au metallization using Z-400 RF sputtering system ➢ Diode configuration three platform and cathodes of 3" diameter target ➢ 04 nos. of 1 sq. inch substrates can be accommodate on each platform in single batch ➢ Ultimate vacuum better than 1x10e-6 Bar. ➢ Process vacuum: 1.0x10e-2 to 4.0x10e-2 Bar. ➢ Argon flow with 2 bar pressure to achieve process vacuum ➢ In situ cleaning by reverse sputtering ➢ Power level: 1.2 kW to 1.6 kW Prior to plating of via hole substrates, abrasive cleaning is critical and required high skills. ➢ Plating: Duty cycle: 20% ± 5% ➢ Ontime: 2 ms. Off time: 8 ms ➢ Average current: 40 to 60 mA (with peak current 0.2 A to 0.6A) ➢ Bath temperature: 55 to 65 deg. C ➢ pH value of bath: 4 ± 0.5
Major Specifications of the Qualified Process	➢ Hole diameter 500 microns ➢ Cr ~300 Angstrom ➢ Au 0.5 to 0.7 microns by sputtering and followed by pulse plating to enhance the thickness ➢ Total metal thickness: 5.0 to 7 microns. ➢ Uniformity of deposited film: ±10% ➢ Contact resistance (ICR): < 0.002 Ω
Photograph	

9. 500 microns hole drilling on 10 mil thick bare Alumina substrates using MS-20 Laser system for via hole metallization	
Salient Features	➢ Hole drilling using MS-20 Laser system ➢ Nd-YAG laser with 1.064 micron wave length ➢ Beam diameter: ~150 microns ➢ Power level: 0.5 W to 2.0W ➢ Pulse repetition rate: 1pulse/sec Burrs cleaning with diamond needle and U/S abrasive power cleaning requires high skills.
Major Specifications of the Qualified Process	➢ 10 mil bare alumina substrates ➢ Total 11 holes in 12.7x12.7 mm square substrates. ➢ Hole diameter 500 microns: ±10% ➢ Location/positioning accuracy: ± 50 microns ➢ Circularity of hole: ±50 microns ➢ Edge flatness: ±50 microns

10. Sub-micron Pattern Generation, CD ≥ 0.75µm, By Lift-off Process, On Quartz SAW Substrate		
Salient Features	The process targets sub-micron pattern definition for high frequency SAW devices (typically for L Band frequencies). Unlike the older process based on wet chemical etching, it employs direct electron beam write and additive metal deposition.	
Major Specifications of the Qualified Process	**Parameters**	**Specifications**
	Wafer Material	Quartz
	Wafer Size / Thickness	3”, 4” diameter / 0.5mm – 2mm
	Pattern	Equal Line / Space (IDT) patterns, CD down to 0.75µm
	Lithography	E-Beam Lithography
	CD Control	±10%
	Evaporation	E-Beam Evaporation System
	Metallization Thickness Range	1000 – 3000A°
	Metallization Thickness Control	±10%
	Metallization Thickness Uniformity	±5% across the wafer
	Pattern Transfer	Lift-Off



11. Photolithography for SAW Pattern Generation. CD= 3µm, Tolerance = ±20% or 3µm, whichever less		
Salient Features	The process targets lithography for wider line dimension SAW devices and is based on wet chemical etching of NiCr and Al.	
Major Specifications of the Qualified Process	**Parameters**	**Specifications**
	Wafer Material	Quartz / $LiNbO_3$
	Wafer Size / Thickness	3", 4" diameter / 0.5mm – 2mm
	Technique	Wet Chemical Etching
	Pattern	Equal Line / Space (IDT) patterns, CD down to 3µm
	Lithography	Photolithography
	CD Control	±20% or 3µm, whichever less
Photograph	Photolithography Qualification Sample 	

12. Double side Patterning of Cr-Au Metalized Substrates using Direct Write LASER (Phase 2)

Salient Features

The process design and developed for front to back alignment (FTBA) with the alignment accuracy +/- 5 micron or better. Circuit critical (CD) dimensions targets 40 micron for high frequency (mm wave) applications. In this process, both sides of substrate patterned using mask-less LASER direct write technique by ensuring proper alignment between the patterns.

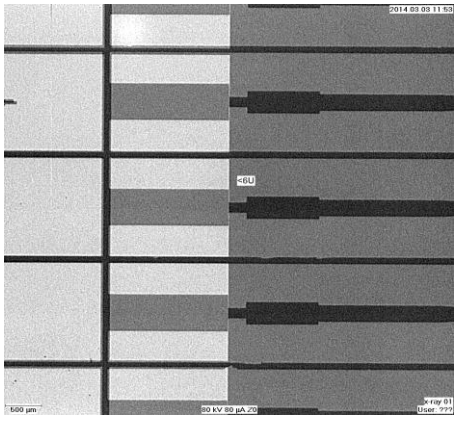
Major Specifications of the Qualified Process

Parameters	Specifications
Substrate Material	Alumina (99.6% or better)
Dielectric Constant	9.8+/-0.1
Substrate Size / Thickness	10 mm-25.4mm/ 254 micron (10 mil)
Pattern	Any shape, line/gap patterns, CD down to 40µm
Lithography	LASER direct write Lithography
Technique	Back Side alignment
CD Control	±10%
Alignment Accuracy	+/- 5 micron
Metallization Scheme	Cr-Au
Metallisation Thickness Range	5-7 micron
Metallisation Thickness Uniformity	±10% across the substrate
Pattern Transfer	Wet etching

Photograph

Top side pattern of mm wave circuit

Bottom side pattern of mm wave circuit



Front to back alignment (FTBA) measurement using X-ray technique

13. Photolithography and Circuit Engraving on In-house Cr-Cu-Au Metalized Substrates (Phase 2)

Salient Features

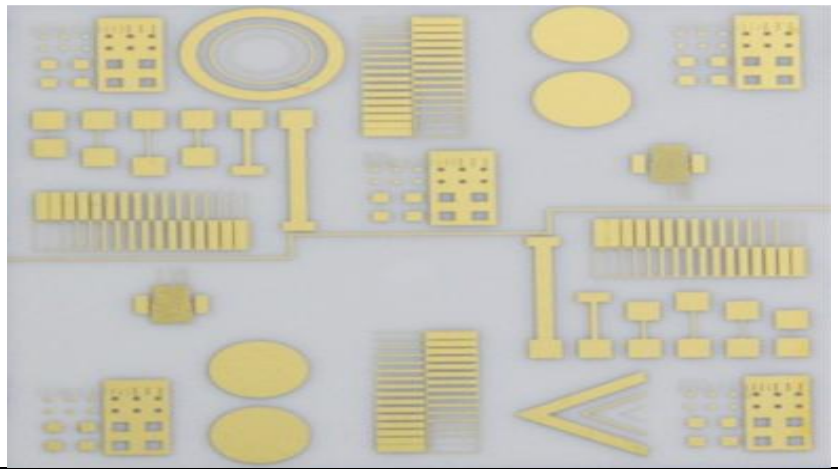
The process developed and parameters optimized for mask based photolithography and circuit engraving. Circuit critical (CD) dimensions targets 100 micron for ongoing communication, Navigation and Remote sensing payloads. In this process, chrome mask/ emulsion mask used to transfer the circuit image on to thin film. Wet chemical etching technique used to get film patterns on to substrate.

Major Specifications of the Qualified Process

Parameters	Specifications
Substrate Material	Alumina (99.6% or better)
Make	In house metalized
Dielectric Constant	9.8+/-0.1
Substrate Size / Thickness	10mm-25.4mm/ 635 micron (25 mil)
Pattern	Any shape, line/gap patterns, CD down to 100µm
Lithography	Photolithography
Mask	Chrome mask/ Emulsion mask
CD Control	±10% or 25 micron whichever is less
Metallization scheme	Cr-Cu-Au
Metallisation Thickness Range	5-7 micron
Metallisation Thickness Control	±10%
Metallisation Thickness Uniformity	±10% across the Substrate
Pattern Transfer	Wet etching

Photograph

Phase-IV pattern used in in-house Cr-Cu-Au qualification



14. Photolithography and Circuit Engraving on M/s UHV metalized, Cr-Cu-Au Metalized Substrates (Phase 2)

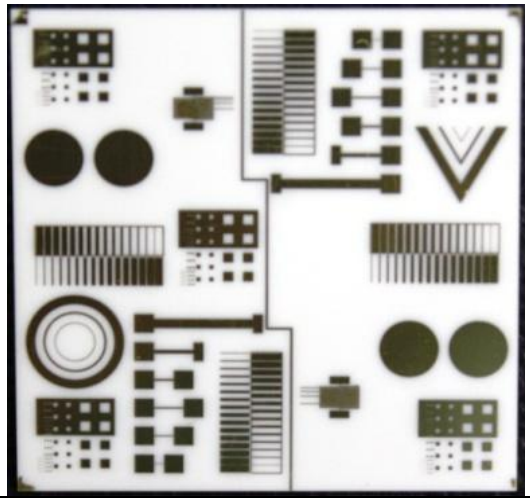
Salient Features

The process design and developed for mask based photolithography and circuit engraving. Circuit critical (CD) dimensions targets 100 micron for ongoing communication, Navigation and Remote sensing payloads. In this process, chrome mask/ emulsion mask used to transfer the circuit image on to thin film. Wet chemical etching technique used to get film patterns on to substrate.

Major Specifications of the Qualified Process

Parameters	Specifications
Substrate Material	Alumina (99.6% or better)
Make	M/s UHV metalized
Dielectric Constant	9.8+/-0.1
Substrate Size / Thickness	10mm-25.4mm/ 635 micron (25 mil)
Pattern	Any shape, line/gap patterns, CD down to 100µm
Lithography	Photolithography
Mask	Chrome mask/ Emulsion mask
CD Control	±10% or 25 micron whichever is less
Metallization scheme	Cr-Cu-Au
Metallisation Thickness Range	5-7 micron
Metallisation Thickness Control	±10%
Metallisation Thickness Uniformity	±10% across the Substrate
Pattern Transfer	Wet etching

Photograph



Phase-IV pattern used in M/s UHV Cr-Cu-Au qualification

15. Direct write LASER Lithography and Circuit Engraving on three layer metalized Alumina substrate

Salient Features

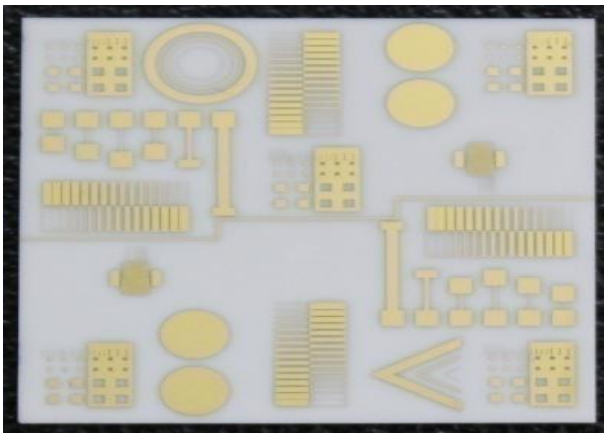
The process design and developed for mask-less direct write LASER lithography and circuit engraving. Circuit critical (CD) dimensions targets 100 micron on three layers (Cr-Cu-Au) for ongoing communication, Navigation and Remote sensing payloads. In this process, CAD data directly write using LASER beam on to resist coated substrate to get circuit image on to thin film. Wet etching technique used to get film patterns on to substrate.

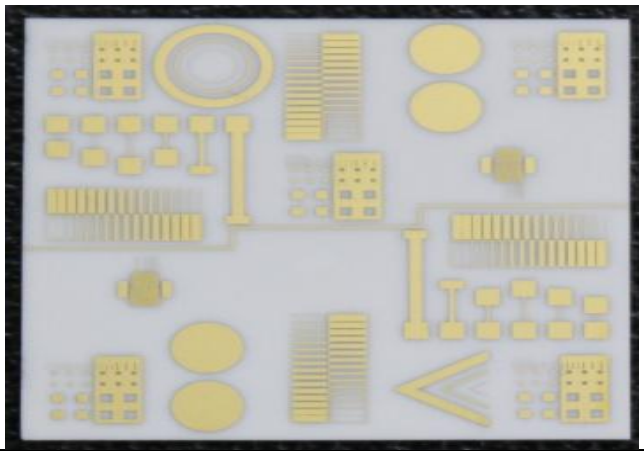
Major Specifications of the Qualified Process

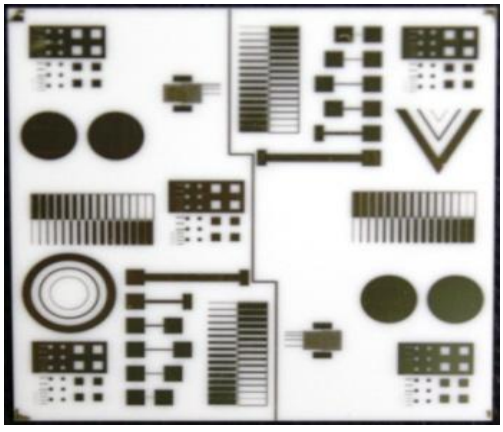
Parameters	Specifications
Substrate Material	Alumina (99.6% or better)
Make	Supplied by MRC, TFT, Materion, USA
Substrate Size / Thickness	10mm-25.4mm/ 635 micron (25 mil)
Pattern	Any shape, line/gap patterns, CD down to 100µm
Lithography	Direct write LASER
Technique	Mask-less
CD Control	±10% or 25 micron whichever is less
Metallization scheme	Cr-Cu-Au
Metallisation Thickness Range	5-7 micron
Metallisation Thickness Control	±10%
Metallisation Thickness Uniformity	±10% across the Substrate
Pattern Transfer	Wet etching

Photograph

Phase-IV pattern used in direct write LASER qualification for three layer metallized substrate



<table>
<tr><th colspan="3">16. Direct write LASER lithography and circuit engraving on two layer metalized Alumina substrate</th></tr>
<tr><td>Salient Features</td><td colspan="2">The process design and developed for mask-less direct write LASER lithography and circuit engraving. Circuit critical (CD) dimensions targets 40 micron on two layers (Cr-Au) for ongoing communication, Navigation and Remote sensing payloads. In this process, CAD data write in serial fashion on to resist coated substrate for transferring the circuit image on to thin film. Wet chemical etching technique used to get film patterns on to substrate.</td></tr>
<tr><td rowspan="13">Major Specifications of the Qualified Process</td><td>Parameters</td><td>Specifications</td></tr>
<tr><td>Substrate Material</td><td>Alumina (99.6% or better)</td></tr>
<tr><td>Make</td><td>In-house metalized</td></tr>
<tr><td>Substrate Size / Thickness</td><td>10mm-25.4mm/ 254 micron (10 mil)</td></tr>
<tr><td>Pattern</td><td>Any shape, line/gap patterns, CD down to 40µm</td></tr>
<tr><td>Lithography</td><td>Direct write LASER</td></tr>
<tr><td>Technique</td><td>Mask-less</td></tr>
<tr><td>CD Control</td><td>±10% or 25 micron whichever is less</td></tr>
<tr><td>Metallization scheme</td><td>Cr-Au</td></tr>
<tr><td>Metallisation Thickness Range</td><td>5-7 micron</td></tr>
<tr><td>Metallisation Thickness Control</td><td>±10%</td></tr>
<tr><td>Metallisation Thickness Uniformity</td><td>±10% across the Substrate</td></tr>
<tr><td>Pattern Transfer</td><td>Wet etching</td></tr>
<tr><td>Photograph</td><td colspan="2">Phase-IV pattern used in direct write LASER qualification for In-house two layer metallized substrate
  </td></tr>
</table>

<table>
<tr><th colspan="3">17. Photo Lithography and Circuit Engraving on two layer metallized Alumina substrate</th></tr>
<tr><td>Salient Features</td><td colspan="2">The process design and developed for mask based photolithography and circuit engraving. Circuit critical (CD) dimensions targets 100 micron for ongoing communication and Remote sensing payloads. In this process, emulsion mask used to transfer the circuit image on to thin film. Wet chemical etching technique used to get film patterns on to substrate.</td></tr>
<tr><td rowspan="13">Major Specifications of the Qualified Process</td><td>Parameters</td><td>Specifications</td></tr>
<tr><td>Substrate Material</td><td>Alumina (99.6% or better)</td></tr>
<tr><td>Make</td><td>In-house metallized</td></tr>
<tr><td>Substrate Size / Thickness</td><td>10mm-25.4mm/ 254 micron (10 mil)</td></tr>
<tr><td>Pattern</td><td>Any shape, line/gap patterns, CD down to 40µm</td></tr>
<tr><td>Lithography</td><td>Photolithography</td></tr>
<tr><td>Mask</td><td>Emulsion mask prepared using photo-reduction technique</td></tr>
<tr><td>CD Control</td><td>±10% or 25 micron whichever is less</td></tr>
<tr><td>Metallization scheme</td><td>Cr-Au</td></tr>
<tr><td>Metallisation Thickness Range</td><td>5-7 micron</td></tr>
<tr><td>Metallisation Thickness Control</td><td>±10%</td></tr>
<tr><td>Metallisation Thickness Uniformity</td><td>±10% across the Substrate</td></tr>
<tr><td>Pattern Transfer</td><td>Wet etching</td></tr>
<tr><td>Photograph</td><td colspan="2">Phase-IV pattern used in Emulsion mask based photolithography for Cr-Au metalized substrate
  </td></tr>
</table>

18. Photo Lithography and Circuit Engraving on three layer metallized Alumina substrate

Salient Features

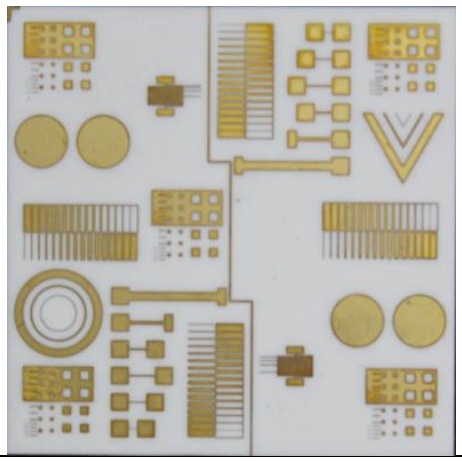
The process design and developed for emulsion mask based photolithography and circuit engraving. Circuit critical (CD) dimensions targets 100 micron for ongoing communication and Remote sensing payloads. In this process, emulsion mask (prepared using photo-reduction technique) used to transfer the circuit image on to thin film. Wet chemical etching technique used to get film patterns on to substrate.

Major Specifications of the Qualified Process

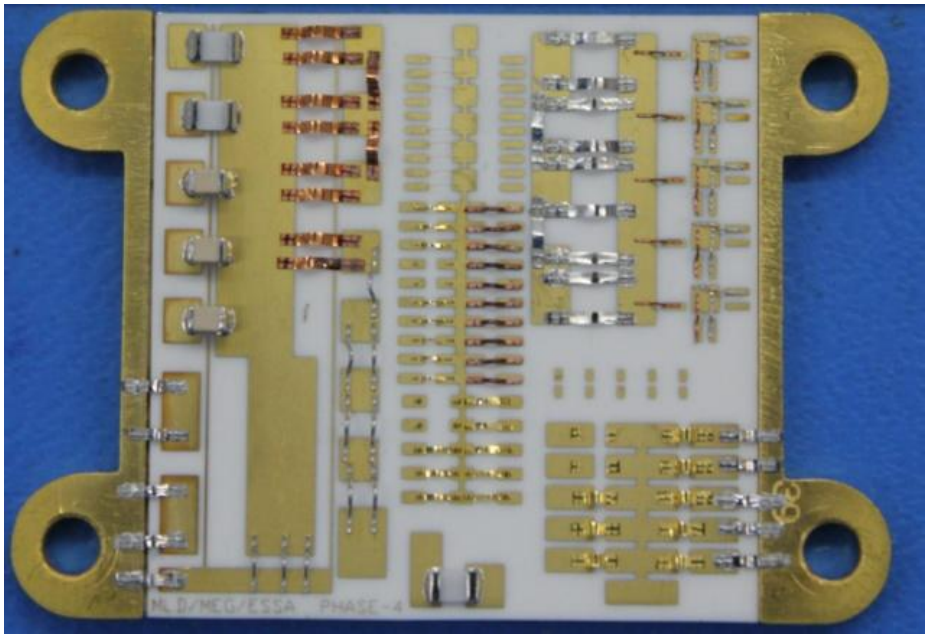
Parameters	Specifications
Substrate Material	Alumina (99.6% or better)
Make	Supplied by MRC, TFT, Materion, USA
Substrate Size / Thickness	10mm-25.4mm/ 635 micron (25 mil)
Pattern	Any shape, line/gap patterns, CD down to 100µm
Lithography	Photolithography
Mask	Emulsion mask prepared using photo-reduction technique
CD Control	±10% or 25 micron whichever is less
Metallization scheme	Cr-Cu-Au
Metallisation Thickness Range	5-7 micron
Metallisation Thickness Control	±10%
Metallisation Thickness Uniformity	±10% across the Substrate
Pattern Transfer	Wet etching

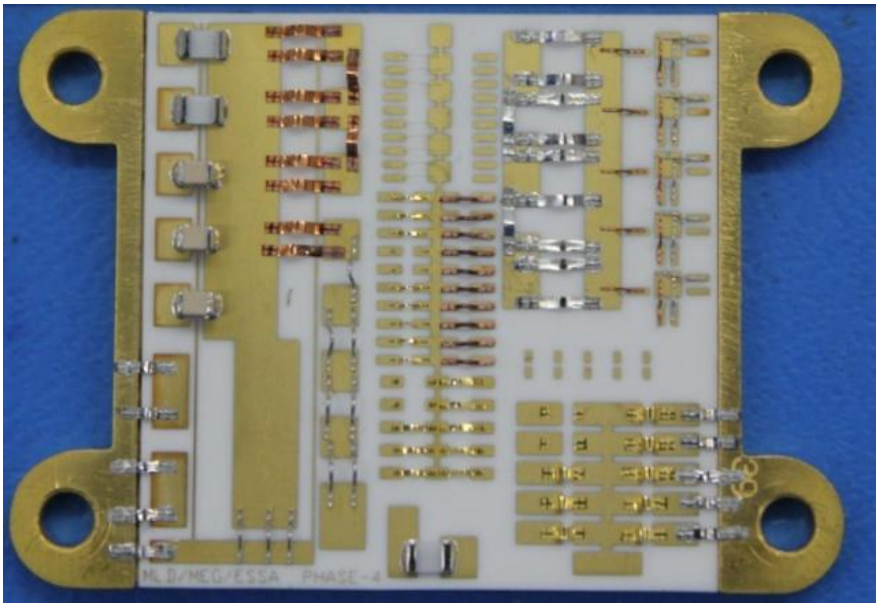
Photograph

Phase-IV pattern used in Emulsion mask based photolithography for Cr-Cu-Au metalized substrate

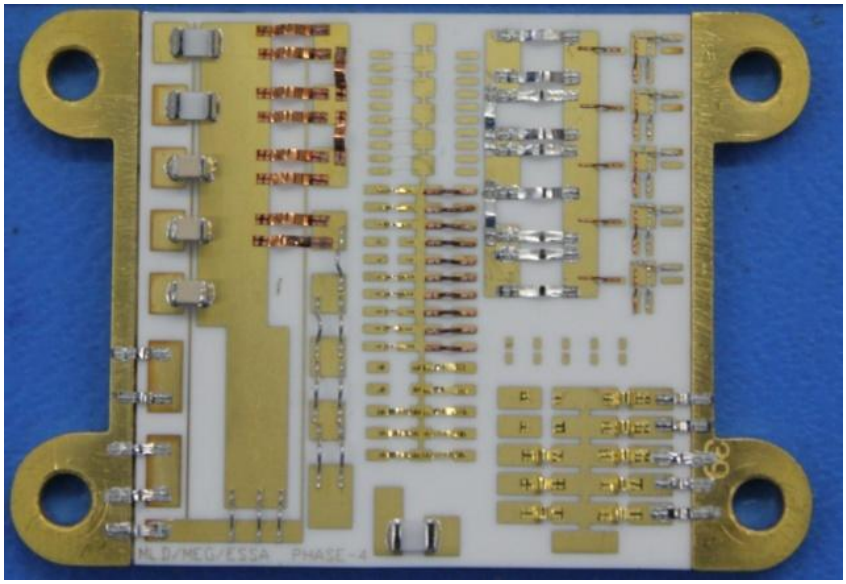


19. Assembly & Packaging of MIC on Alumina

Introduction	Three layers (Cr-Cu-Au) & Two layer (Cr-Au) metalized alumina substrates have been assembled & qualified prior to use in FM hardware samples were processed for MIC Assembly Processes for qualification testing.		
Major Specifications of the Qualified Process	**Salient Features**	**Technology**	**Feature Size**
	Substrate Type	Alumina	
	Substrate Size	1"X1", 25mil, 10mil	Three & two layer
	Attachment Process	Reflow process	Solder Preform Au/Sn 80/ 20
	Component Type & attachment Process	SMD, Reflow , Hot Gas & hand soldering process	Sn/Pb/Ag 62/36/2
	Gold Ribbon Bonding	Parallel Gap Bonding	20mil, 10mil, 5mil
	Gold Wire Bonding	Parallel Gap Bonding	1mil
	Epoxy (Conductive & Non Conductive)	Manual	H81 , H74
Photograph			

<table>
<tr><th colspan="4">20. MIC Assembly Processes on Metallized Alumina Substrate of M/s UHV Sputtering</th></tr>
<tr><td>Introduction</td><td colspan="3">Three layers (Cr-Cu-Au) metallized alumina substrates have been procured for the first time from M/s UHV Sputtering, U.S.A. by TSPD/MEG/ESSA. Hence, prior to use in FM hardware samples were processed for MIC Assembly Processes (as per Phase –IV, ISRO PAX-305) for qualification testing.</td></tr>
<tr><td rowspan="8">Major Specifications of the Qualified Process</td><td>Salient Features</td><td>Technology</td><td>Feature Size</td></tr>
<tr><td>Substrate Type</td><td>Alumina</td><td></td></tr>
<tr><td>Substrate Size</td><td>1”X1”, 25mil</td><td>Three layer Cr-Cu-Au</td></tr>
<tr><td>Attachment Process</td><td>Reflow process</td><td>Solder Preform Au/Sn 80/ 20</td></tr>
<tr><td>Component Type & attachment Process</td><td>SMD, Reflow , Hot Gas & hand soldering process</td><td>Sn/Pb/Ag 62/36/2</td></tr>
<tr><td>Gold Ribbon Bonding</td><td>Parallel Gap Bonding</td><td>20mil, 10mil, 5mil</td></tr>
<tr><td>Gold Wire Bonding</td><td>Parallel Gap Bonding</td><td>1mil</td></tr>
<tr><td>Epoxy (Conductive & Non Conductive)</td><td>Manual</td><td>H81 , H74</td></tr>
<tr><td>Photograph</td><td colspan="3">  </td></tr>
</table>

21. MIC Assembly Processes on In-house Metalized Alumina Substrate

	Salient Feature	Technology	Feature Size
Major Specifications of the Qualified Process	Substrate Type	Alumina	
	Substrate Size	1"X1", 25mil	Three layer Cr-Cu-Au
	Attachment Process	Reflow process	Solder Preform Au/Sn 80/ 20
	Component Type & attachment Process	SMD, Reflow , Hot Gas & hand soldering process	Sn/Pb/Ag 62/36/2
	Gold Ribbon Bonding	Parallel Gap Bonding	20mil, 10mil, 5mil
	Gold Wire Bonding	Parallel Gap Bonding	1mil
	Epoxy (Conductive & Non Conductive)	Manual	H81 , H74
Photograph			

22. MIC Assembly Process on SILVAR Carrier Plate

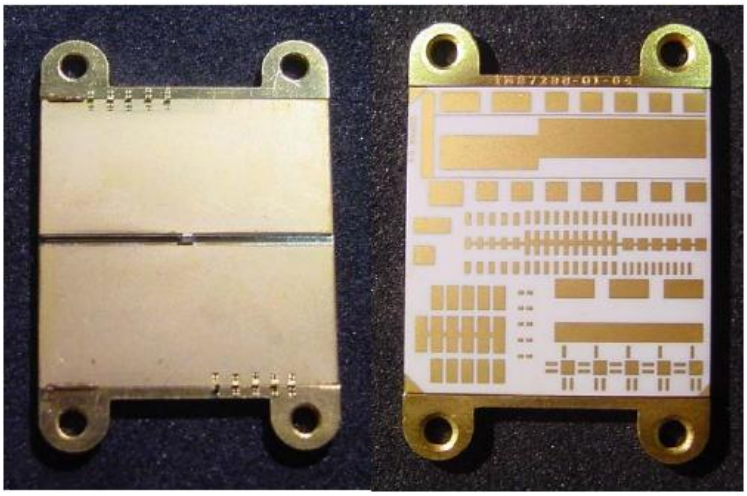
Introduction

SILVAR carrier plates are being planned to use in future Microwave Integrated Circuits (MICs) subsystem for high power applications. It provides "high thermal conductivity and thermal expansion coefficient matching with Alumina as well as GaAs. Since substrate & bare die attachment, gold wire/ribbon bonding and gold epoxy application to gold-plated SILVAR carrier plate are new processes, it is essential to evaluate & qualify the processes before starting FM fabrication.

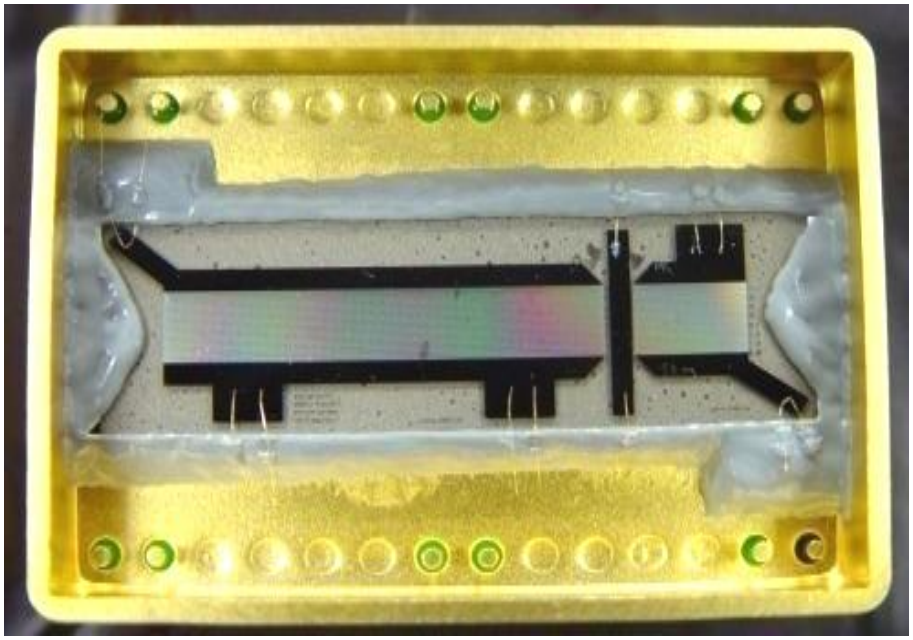
Major Specifications of the Qualified Process

Salient Feature	Technology	Feature Size
Substrate Type	Alumina	
Substrate Size	1"X1", ½"X1" 25mil	Three layer Cr-Cu-Au
Attachment Process	Reflow process	Solder Preform Au/Sn 80/ 20
MMIC Attachment	Reflow process	Solder Preform Au/Sn 80/ 20
Component Type & attachment Process	SMD, Reflow , Hot Gas & hand soldering process	Sn/Pb/Ag 62/36/2
Gold Ribbon Bonding	Parallel Gap Bonding	20mil, 10mil, 5mil
Gold Wire Bonding	Parallel Gap Bonding	1mil
Epoxy (Conductive & Non Conductive)	Manual	H81 , H74

Photograph



23. Assembly & Packaging of SAW devices

Introduction	Surface Acoustic Wave (SAW) is used for convert RF signal to SAW & vice versa. The SAW device is very brittle having aluminum metallization. The assembly of SAW substrate and gold wire bond between SAW & gold plated Package is qualified process for space Use.		
Major Specifications of the Qualified Process	**Salient Feature**	**Technology**	**Feature Size**
	Substrate Type	Quartz & $LiNbO_3$ and $LiTao_3$	
	Package Size	1”x1” min &1”x3”max, height 0.4” to 1”	
	Attachment Process	Epoxy Application	Conductive Epoxy RTV 1075
	Gold Wire Bonding	Parallel Gap Bonding	1mil
	RTV application	Manual	RTV3145
Photograph			

24. Kovar Hybrid Assembly Process using Alumina Substrate (Direct attach)

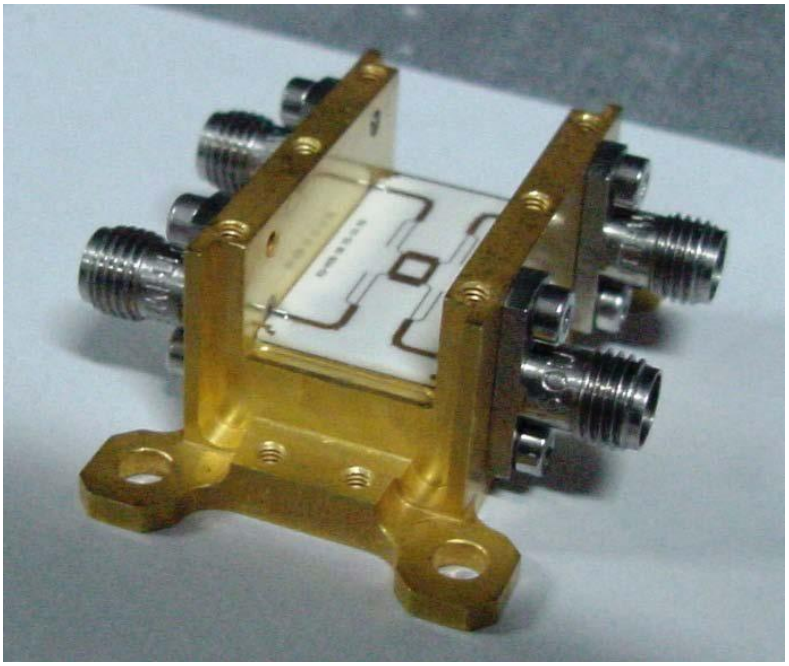
Introduction

Hybrid circuits are used at various places in payload as an integration component or as a part of subsystem. The Hybrid is used after receivers to connect main and redundant receivers to the even and odd Input Multiplexers. The hybrid is fabricated using substrate attached on carrier plate & carrier plate assembly in actual package. In this new process MIC substrate directly attached on gold plated Kovar package. With this process, size of whole circuit can be reduced and electrical performance can also be improved.

Major Specifications of the Qualified Process

Salient Feature	Technology	Feature Size
Substrate Type	Alumina	
Substrate Size	1"X ½" , 25mil & 10mil	Three layer Cr-Cu-Au
Attachment Process	Reflow process	Solder Preform Au/Sn 80/ 20
Component Type & attachment Process	SMD, Reflow , Hot Gas & hand soldering process	Sn/Pb/Ag 62/36/2

Photograph



25. Duroid Assembly & Packaging of RT-Duroid 6002

Introduction

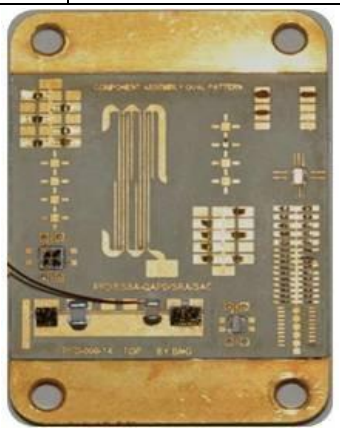
Gold plated Duroid substrate are planned to be used in future subsystem for high power applications. The RF subsystems for communication & earth observation payloads like GSAT-11, GISAT, etc. are to be realized using these laminates of various thickness & sizes. The development of these types of payloads/subsystems requires following microwave assembly processes to be qualified on Duroid substrates

a) Attachment of Duroid substrate to Kovar carrier plate
b) Component mounting & soldering on Duroid
c) Gold Wire and ribbon bonding on Duroid
d) Single layer multi-capacitor Chip mounting and wire bonding
e) Gold epoxy application on Duroid

Major Specifications of the Qualified Process

Salient Feature	Technology	Feature Size
Substrate Type	RT-Duroid 6002	
Substrate Size	1"X1", 10mil	½ Oz Metallization
Attachment Process	Reflow process	Sn/Pb/Ag 62/36/2
MMIC Attachment	Manual	Silver Epoxy
Component Type & attachment Process	SMD, Hot Gas & hand soldering process	Sn/Pb/Ag 62/36/2
Gold Ribbon Bonding	Parallel Gap Bonding	20mil, 10mil, 5mil
Gold Wire Bonding	Parallel Gap Bonding, wedge bonding	1mil
Epoxy Gold &Silver	Manual	H81 , H21D

Photograph



26. Duroid Assembly & Packaging of RT-Duroid 6010

Introduction

Gold plated Duroid substrate are planned to be used in future subsystem for high power applications. The RF subsystems for communication & earth observation payloads like GSAT-11, GISAT, etc. are to be realized using these laminates of various thickness & sizes. The development of these types of payloads/sub systems requires following microwave assembly processes to be qualified on Duroid substrates

a) Attachment of Duroid substrate to Kovar carrier plate
b) Component mounting & soldering on Duroid
c) Gold Wire and ribbon bonding on Duroid
d) Single layer multi-capacitor Chip mounting and wire bonding
e) Gold epoxy application on Duroid

Major Specifications of the Qualified Process

Salient Feature	Technology	Feature Size
Substrate Type	RT-Duroid 6010	
Substrate Size	1"X1", 25mil	½ Oz metallization
Attachment Process	Reflow process	Sn/Pb/Ag 62/36/2
MMIC Attachment	Manual	Silver Epoxy
Component Type & attachment Process	SMD, Hot Gas & hand soldering process	Sn/Pb/Ag 62/36/2
Gold Ribbon Bonding	Parallel Gap Bonding	20mil, 10mil, 5mil
Gold Wire Bonding	Parallel Gap Bonding, wedge bonding	1mil
Epoxy Gold &Silver	Manual	H81 , H21D

Photograph

27. Duroid Assembly & Packaging of RT-Duroid 6010 with cu back

Introduction

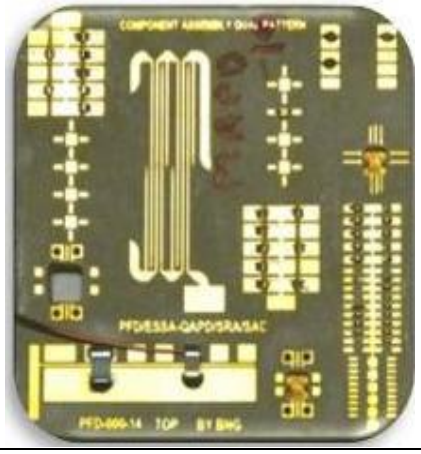
Gold plated Duroid substrate are planned to be used in future subsystem for high power applications. The RF subsystems for communication & earth observation payloads like GSAT-11, GISAT, etc. are to be realized using these laminates of various thickness & sizes. The development of these types of payloads/sub systems requires following microwave assembly processes to be qualified on Duroid substrates

a) Component mounting & soldering on Duroid
b) Gold Wire and ribbon bonding on Duroid
c) Single layer multi-capacitor Chip mounting and wire bonding
d) Gold epoxy application on Duroid

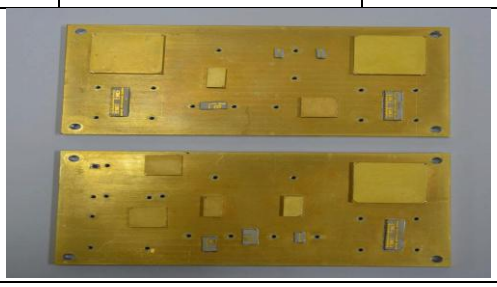
Major Specifications of the Qualified Process

Salient Feature	Technology	Feature Size
Substrate Type	RT-Duroid 6010 with Cu Back	
Substrate Size	1"X1", 25mil	½ Oz metallization
Component Type & attachment Process	SMD, Hot Gas & hand soldering process	Sn/Pb/Ag 62/36/2
Gold Ribbon Bonding	Parallel Gap Bonding	20mil, 10mil, 5mil
Gold Wire Bonding	Parallel Gap Bonding,	1mil
Epoxy Gold	Manual	H81

Photograph



29. Assembly Process on Double Side Patterned, 10 mil thick Alumina (Cr-Au) MIC			
Introduction	Assembly Process on Double Side Patterned, 10 mil Thick Two Layer (Cr-Au) Metallized Alumina Substrate (Cantilever Configuration) RF Transition used in SCATSAT-1 FESA LNA.		
Major Specifications of the Qualified Process	**Salient Feature**	**Technology**	**Feature Size**
	Substrate Type	Alumina	10mil thick
	Substrate Size	2.56mmx8.5mm	Two layer Cr-Au
	Attachment Process	Reflow process	Solder Preform Au/Sn 80/ 20
	Gold Ribbon Bonding	Parallel Gap Bonding	10mil, 5mil

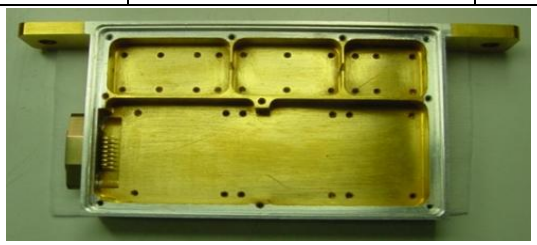
30. The epoxy-attach processes using Epotek H21D - **Cu-back Duroid to Gold-plated Aluminium** **31.** The epoxy-attach processes using Epotek H21D - **Substrate attached Kovar plate to Kovar.**			
Introduction	The Ku & Ka band converter realization for GSAT-11 requires direct attachment of, 1) Cu-back Duroid on to gold-plated Aluminium packages & 2) Kovar Carrier (with substrate) on Gold-plated Kovar. In these processes, the attachments are to be carried out using Epotek H21D silver epoxy. Since these processes are being proposed for first time for space-use, it is essential to qualify prior to FM fabrication. The testing has been carried out on the samples, fabricated by MAPD/MEG/SRA.		
Major Specifications of the Qualified Process	**Salient Feature**	**Technology**	**Feature Size**
	Substrate Type	Cu-back Duroid	3.0 x 6.4 to 19.5 x 6.3
	Plate	Kovar	12.7 x 6.3 to 25.4 x 25.4
	Epoxy Silver	Manual	H21D
Photograph			

32. Incremental Process Qualification using Solder & Epoxy

Introduction	To meet project requirements in GSAT-16, it was planned to use HMC based control circuit for ALC DA. The PFT-substrate assembled at M/s Centum. While the post-optimization device assembly and wiring of this control circuit shall be completed at SAC. The HMC based control circuits are to be integrated in the ALC-DA package in-house and new processes are envisaged for the realization of control circuit of ALC DA are, Attachment of MMIC chip by silver epoxy, Cu-magnet wire soldering on HMC, Micro-D connector interconnections using Cu-magnet wire soldering, Component attachment using silver epoxy (Epotek H-21D).		
Major Specifications of the Qualified Process	**Salient Feature**	**Technology**	**Feature Size**
	Substrate Type	PFT	
	Cu-magnet wire solder	Hot Gas & hand soldering process	Sn/Pb/Ag 62/36/2
	Component attachment	Manual	Silver Epoxy
	Epoxy Silver	Manual	H81 , H21D

33. Hermetic sealing process of Gold plated Al packages using laser welding of cover (Butt joint) and soldered DC & RF Feed-through

Introduction	Hermetic sealing process of Gold plated Al Package using laser welding of cover (butt joint) qualified process for space Use.		
Major Specifications of the Qualified Process	**Salient Feature**	**Technology**	**Feature Size**
	Box Al6061, lid Al4047	Laser Hermetic sealing	Laser type Nd YAG wavelength 1064nm
	Box Size	125x45x25mm	-
	RF bead and DC feedthru attachment	Solder process	-
Photograph			

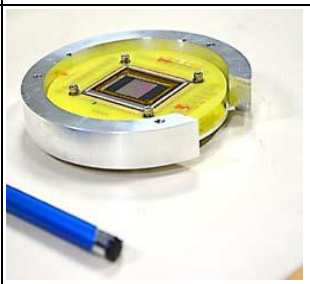
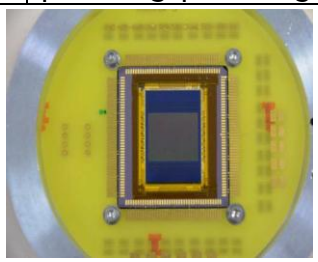
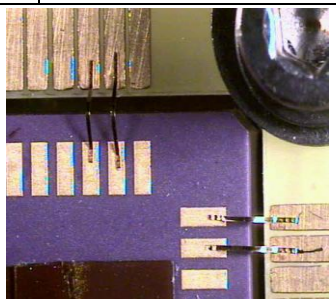
34. Hermetic sealing process of Micro D Connector with Gold plated Al packages using Laser Welding			
Introduction	Hermetic sealing process of Micro D connector with Gold plated Al Package using laser welding qualified process for space Use.		
Major Specifications of the Qualified Process	**Salient Feature**	**Technology**	**Feature Size**
	Box Al6061, MicroD connector outershell Al4047	Laser Hermetic sealing	Laser type Nd YAG wavelength 1064nm
	Box Size	70x45x25mm	-
Photograph			

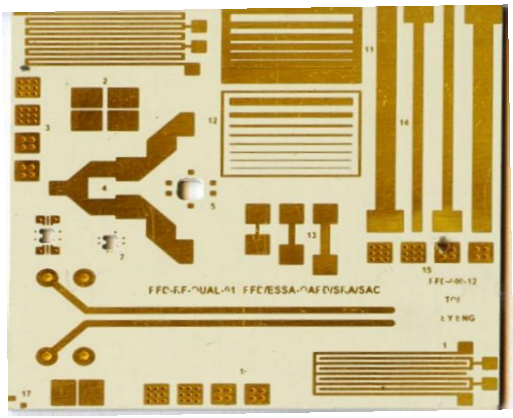
35. Hermetic sealing of Laser weldable RF connectors & DC feed through Hermetic with Al packages using Laser Welding			
Introduction	Hermetic sealing process of Micro D connector with Gold plated Al Package using laser welding qualified process for space Use.		
Major Specifications of the Qualified Process	**Salient Feature**	**Technology**	**Feature Size**
	Box Al6061, laser weldable RF connector & DC feedthrough. Outer shell Al4047	Laser Hermetic sealing	Laser type Nd YAG wavelength 1064nm
	Box Size	45x45x25mm	-
Photograph			

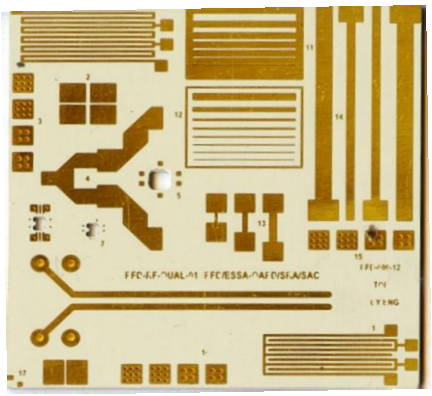
36. Laser welding of cover by Lap fillet type joint

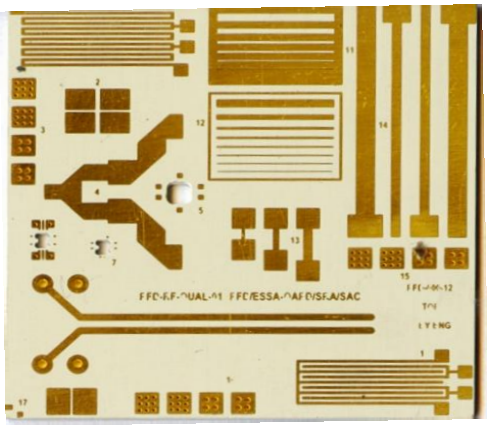
Introduction	Hermetic sealing process of Micro D connector with Gold plated Al Package using laser welding qualified process for space use.		
Major Specifications of the Qualified Process	**Salient Feature**	**Technology**	**Feature Size**
	Box Al6061, lidAl4047	Laser Hermetic sealing	Laser type Nd YAG wavelength 1064nm
	Box Size	45x45x25mm	-
Photograph			

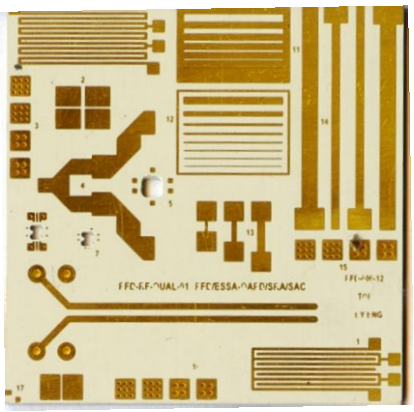
37. Gold plated FR-4 PCB, 5mil Ribbon Bonding Process for Detector cleared for ASTROSAT UVIT only

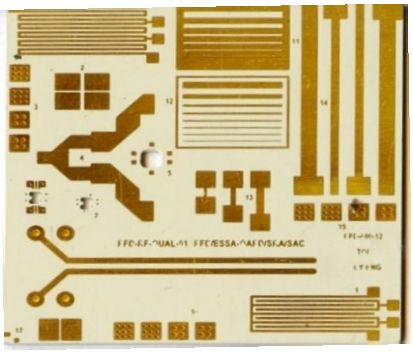
Introduction	This is with reference to meeting held on in May, 2014 for evaluation of gold ribbon bonding for making interconnection of CIS2051 Detector to gold-plated FR4 PCBs. An exercise has been carried out with one detector bonded on metal plate and interconnections are made through 5-mil ribbon bonds.		
Major Specifications of the Qualified Process	**Salient Feature**	**Technology**	**Feature Size**
	Substrate Type	Gold plated FR4 PCB	Supplied by PFD/ESSA
	Package with attached Detector	168-pin CIS2051 Detector (Electrically non-functional)	Assembled supplied by project.
	Interconnection	5mil ribbon bonding, parallel gap bonding	MAPD/ESSA
Photograph	  		

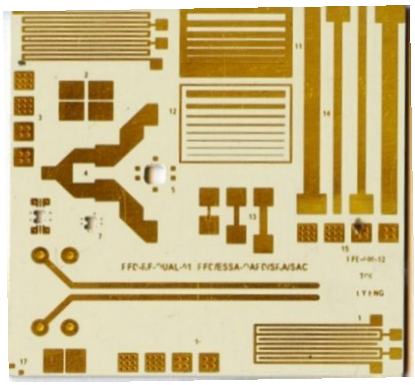
<table>
<tr><th colspan="3">38. PTH and Pattern generation with Gold finished PCBs on RT Duroid 6002 having laminate thickness 10 mil & ¼ Oz basic Copper</th></tr>
<tr><td>Salient Features</td><td colspan="2">Drilling of 10 mil thick RT Duroid 6010 laminate with ¼ Oz basic Cu is being done on high speed CNC drilling machine followed by the PTFE activation, PTH process and soft gold plating. After image transfer by using a negative photo film, gold and copper etching is carried out under the controlled condition to ensure minimum overhang and 130 micron lines and spacing can be achieved on a total minimum 50 micron copper thickness. Slot making and routing process is being carried out for the required size on CNC drilling machine.</td></tr>
<tr><td>Qualification test plan</td><td colspan="2">SAC/SRA/GEN/PQP/12.0/July 2013, Qualification Test plan for Gold plating / Solder Coating (using HAL) & pattern Generation Process of PCB fabrication with PTH on PTFE laminates.</td></tr>
<tr><td rowspan="10">Qualification Specifications</td><td>Description</td><td>Requirements</td></tr>
<tr><td>Laminate Type</td><td>RT-6002</td></tr>
<tr><td>Laminate Thickness</td><td>10 mil</td></tr>
<tr><td>Basic Copper thickness</td><td>¼ oz (8 µm)</td></tr>
<tr><td>Type of Finish</td><td>Gold finish</td></tr>
<tr><td>Track width / Spacing (min)</td><td>0.12 mm</td></tr>
<tr><td>Gold plating Thickness (min)</td><td>2 µm (2 to 8 µm)</td></tr>
<tr><td>Hole Size (min)</td><td>0.3mm</td></tr>
<tr><td>Gold plating thickness in PTH</td><td>2 to 15 µm</td></tr>
<tr><td>Slot size (min)</td><td>0.8 x 1.5 mm</td></tr>
<tr><td>Photograph</td><td colspan="2">  </td></tr>
</table>

<table>
<tr><th colspan="3">39. PTH and Pattern generation with Gold finished PCBs on RT Duroid 6010 having laminate thickness 25 mil & ½ Oz basic Copper</th></tr>
<tr><td>Salient Features</td><td colspan="2">Drilling of 25 mil thick RT Duroid 6010 laminate with ½ Oz basic Cu is being done on high speed CNC drilling machine followed by the PTFE activation, PTH process and soft gold plating. After image transfer by using a negative photo film, gold and copper etching is carried out under the controlled condition to ensure minimum overhang and 130 micron lines and spacing can be achieved on a total minimum 50 micron copper thickness. Slot making and routing process is being carried out for the required size on CNC drilling machine.</td></tr>
<tr><td>Qualification test plan</td><td colspan="2">SAC/SRA/GEN/PQP/12.0/July 2013, Qualification Test plan for Gold plating / Solder Coating (using HAL) & pattern Generation Process of PCB fabrication with PTH on PTFE laminates.
PID No.: SAC\ESSA\EFMG\PFD\PID\01\MARCH, 2014</td></tr>
<tr><td rowspan="10">Qualification Specifications</td><td>Description</td><td>Requirements</td></tr>
<tr><td>Laminate Type</td><td>RT-6010</td></tr>
<tr><td>Laminate Thickness</td><td>25 mil</td></tr>
<tr><td>Basic Copper thickness</td><td>½ oz (17 µm)</td></tr>
<tr><td>Type of Finish</td><td>Gold finish</td></tr>
<tr><td>Track width / Spacing (min)</td><td>0.12 mm</td></tr>
<tr><td>Gold plating Thickness (min)</td><td>2 µm (2 to 8 µm)</td></tr>
<tr><td>Hole Size (min)</td><td>0.3mm</td></tr>
<tr><td>Gold plating thickness in PTH</td><td>2 to 15 µm</td></tr>
<tr><td>Slot size (min)</td><td>0.8 x 1.5 mm</td></tr>
<tr><td>Photograph</td><td colspan="2">  </td></tr>
</table>

<table>
<tr><th colspan="3">40. PTH and Pattern generation with Gold finished PCBs on RT Duroid 6010 having laminate thickness 20 mil & ¼ Oz basic Copper</th></tr>
<tr><td>Salient Features</td><td colspan="2">Drilling of 20 mil thick RT Duroid 6010 laminate with ¼ Oz basic Cu is being done on high speed CNC drilling machine followed by the PTFE activation, PTH process and soft gold plating. After image transfer by using a negative photo film, gold and copper etching is carried out under the controlled condition to ensure minimum overhang and 130 micron lines and spacing can be achieved on a total minimum 50 micron copper thickness. Slot making and routing process is being carried out for the required size on CNC drilling machine.</td></tr>
<tr><td>Qualification test plan</td><td colspan="2">SAC/SRA/GEN/PQP/12.0/July 2013, Qualification Test plan for Gold plating / Solder Coating (using HAL) & pattern Generation Process of PCB fabrication with PTH on PTFE laminates.
PID No.: SAC\ESSA\EFMG\PFD\PID\01\MARCH, 2014</td></tr>
<tr><td rowspan="10">Qualification Specifications</td><td>Description</td><td>Requirements</td></tr>
<tr><td>Laminate Type</td><td>RT-6010</td></tr>
<tr><td>Laminate Thickness</td><td>20 mil</td></tr>
<tr><td>Basic Copper thickness</td><td>¼ oz (8 µm)</td></tr>
<tr><td>Type of Finish</td><td>Gold finish</td></tr>
<tr><td>Track width / Spacing (min)</td><td>0.12 mm</td></tr>
<tr><td>Gold plating Thickness (min)</td><td>2 µm (2 to 8 µm)</td></tr>
<tr><td>Hole Size (min)</td><td>0.3mm</td></tr>
<tr><td>Gold plating thickness in PTH</td><td>2 to 15 µm</td></tr>
<tr><td>Slot size (min)</td><td>0.8 x 1.5 mm</td></tr>
<tr><td>Photograph</td><td colspan="2">  </td></tr>
</table>

<table>
<tr><th colspan="3">41. PTH and Pattern generation with Gold finished PCBs on RT Duroid 6002 having laminate thickness 10mil & ¼ Oz basic copper and 1mm Cu backup</th></tr>
<tr><td>Salient Features</td><td colspan="2">Drilling of 10 mil thick RT Duroid 6002 laminate with ¼ Oz basic Cu & 1 mm thick copper backup is being done on high speed CNC drilling machine by using a pack drilling method followed by the PTFE activation, PTH process and soft gold plating. After image transfer by using a negative photo film, gold and copper etching is carried out under the controlled condition which ensures minimum overhang and 130 micron lines and spacing can be achieved on a total minimum 50 micron copper thickness. Slot making and routing process is being carried out for the required size on CNC drilling machine.</td></tr>
<tr><td>Qualification test plan</td><td colspan="2">SAC/SRA/GEN/PQP/12.0/July 2013, Qualification Test plan for Gold plating / Solder Coating (using HAL) & pattern Generation Process of PCB fabrication with PTH on PTFE laminates.
PID No.: SAC\ESSA\EFMG\PFD\PID\02\JULY, 2015</td></tr>
<tr><td rowspan="10">Qualification Specifications</td><td>Description</td><td>Requirements</td></tr>
<tr><td>Laminate Type</td><td>RT-6002 with 1mm copper backup</td></tr>
<tr><td>Laminate Thickness</td><td>10 mil</td></tr>
<tr><td>Basic Copper thickness</td><td>¼ oz (8 µm)</td></tr>
<tr><td>Type of Finish</td><td>Gold finish</td></tr>
<tr><td>Track width / Spacing (min)</td><td>0.12 mm</td></tr>
<tr><td>Gold plating Thickness (min)</td><td>2 µm (2 to 8 µm)</td></tr>
<tr><td>Hole Size (min)</td><td>0.5mm</td></tr>
<tr><td>Gold plating thickness in PTH</td><td>2 to 15 µm</td></tr>
<tr><td>Slot size (min)</td><td>0.8 x 1.5 mm</td></tr>
<tr><td>Photograph</td><td colspan="2">  </td></tr>
</table>

<table>
<tr><th colspan="3">42. PTH and Pattern generation with Gold finished PCBs on RT Duroid 6002 having laminate thickness 20 mil & ¼ Oz basic Copper and 1mm Cu backup</th></tr>
<tr><td>Salient Features</td><td colspan="2">Drilling of 20 mil thick RT Duroid 6002 laminate with ¼ Oz basic Cu & 1 mm thick copper backup is being done on high speed CNC drilling machine by using a pack drilling method followed by the PTFE activation, PTH process and soft gold plating. After image transfer by using a negative photo film, gold and copper etching is carried out under the controlled condition which ensures minimum overhang and 130 micron lines and spacing can be achieved on a total minimum 50 micron copper thickness. Slot making and routing process is being carried out for the required size on CNC drilling machine.</td></tr>
<tr><td>Qualification test plan</td><td colspan="2">SAC/SRA/GEN/PQP/12.0/July 2013, Qualification Test plan for Gold plating / Solder Coating (using HAL) & pattern Generation Process of PCB fabrication with PTH on PTFE laminates.
PID No.: SAC\ESSA\EFMG\PFD\PID\02\JULY,2015</td></tr>
<tr><td rowspan="10">Qualification Specifications</td><td>Description</td><td>Requirements</td></tr>
<tr><td>Laminate Type</td><td>RT-6002 with 1mm copper backup</td></tr>
<tr><td>Laminate Thickness</td><td>20 mil</td></tr>
<tr><td>Basic Copper thickness</td><td>¼ oz (8 µm)</td></tr>
<tr><td>Type of Finish</td><td>Gold finish</td></tr>
<tr><td>Track width / Spacing (min)</td><td>0.12 mm</td></tr>
<tr><td>Gold plating Thickness (min)</td><td>2 µm (2 to 8 µm)</td></tr>
<tr><td>Hole Size (min)</td><td>0.5mm</td></tr>
<tr><td>Gold plating thickness in PTH</td><td>2 to 15 µm</td></tr>
<tr><td>Slot size (min)</td><td>0.8 x 1.5 mm</td></tr>
<tr><td>Photograph</td><td colspan="2">  </td></tr>
</table>

<table>
<tr><th colspan="3">43. PTH and Pattern generation with Gold finished PCBs on RT Duroid 6002 having laminate thickness 20 mil & ½ Oz basic Copper and 1mm Cu backup</th></tr>
<tr><td>Salient Features</td><td colspan="2">Drilling of 20 mil thick RT Duroid 6002 laminate with ½ Oz basic Cu & 1 mm thick copper backup is being done on high speed CNC drilling machine by using a pack drilling method followed by the PTFE activation, PTH process and soft gold plating. After image transfer by using a negative photo film, gold and copper etching is carried out under the controlled condition which ensures minimum overhang and 130 micron lines and spacing can be achieved on a total minimum 50 micron copper thickness. Slot making and routing process is being carried out for the required size on CNC drilling machine.</td></tr>
<tr><td>Qualification test plan</td><td colspan="2">SAC/SRA/GEN/PQP/12.0/July 2013, Qualification Test plan for Gold plating / Solder Coating (using HAL) & pattern Generation Process of PCB fabrication with PTH on PTFE laminates.
PID No.: SAC\ESSA\EFMG\PFD\PID\02\JULY,2015</td></tr>
<tr><td rowspan="10">Qualification Specifications</td><td>Description</td><td>Requirements</td></tr>
<tr><td>Laminate Type</td><td>RT-6002 with 1mm copper backup</td></tr>
<tr><td>Laminate Thickness</td><td>10 mil</td></tr>
<tr><td>Basic Copper thickness</td><td>½ oz (17 µm)</td></tr>
<tr><td>Type of Finish</td><td>Gold finish</td></tr>
<tr><td>Track width / Spacing (min)</td><td>0.12 mm</td></tr>
<tr><td>Gold plating Thickness (min)</td><td>2 µm (2 to 8 µm)</td></tr>
<tr><td>Hole Size (min)</td><td>0.3mm</td></tr>
<tr><td>Gold plating thickness in PTH</td><td>2 to 15 µm</td></tr>
<tr><td>Slot size (min)</td><td>0.8 x 1.5 mm</td></tr>
<tr><td>Photograph</td><td colspan="2">  </td></tr>
</table>

44. PTH and Pattern generation with Gold finished PCBs on CLTE XT having laminate thickness 20 mil & ½ Oz basic Copper

Salient Features

Drilling of 20 mil thick RT6002 laminate with ½ Oz basic Cu is being done on high speed CNC drilling machine followed by the PTFE activation, PTH process and soft gold plating. After image transfer by using a negative photo film, gold and copper etching is carried out under the controlled condition which ensures minimum overhang and 130 micron lines and spacing can be achieved on a total minimum 50 micron copper thickness. Slot making and routing process is being carried out for the required size on CNC drilling machine.

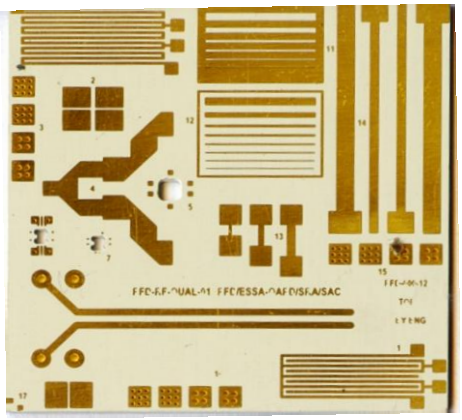
Qualification test plan

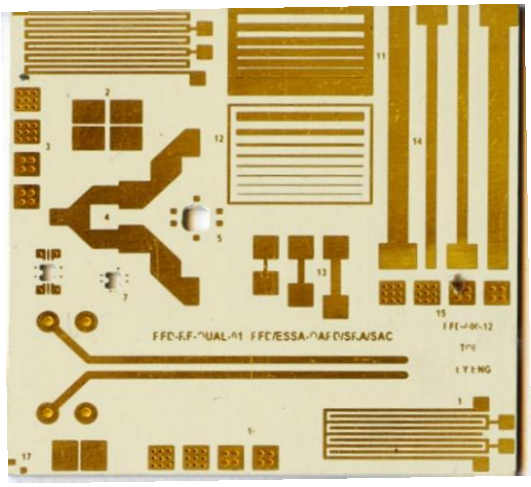
SAC/SRA/GEN/PQP/12.0/July 2013, Qualification Test plan for Gold plating / Solder Coating (using HAL) & pattern Generation Process of PCB fabrication with PTH on PTFE laminates.
PID No.: SAC\ESSA\EFMG\PFD\PID\01\MARCH, 2014

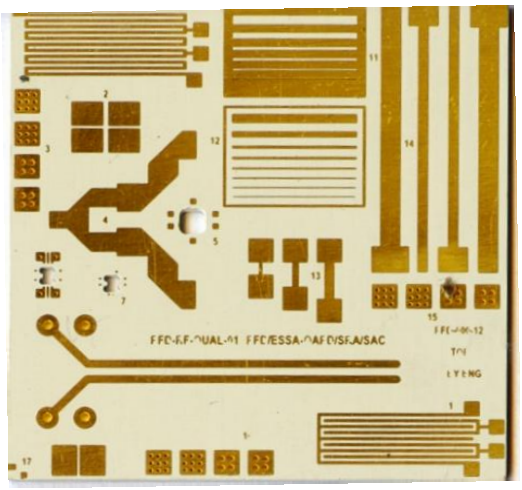
Qualification Specifications

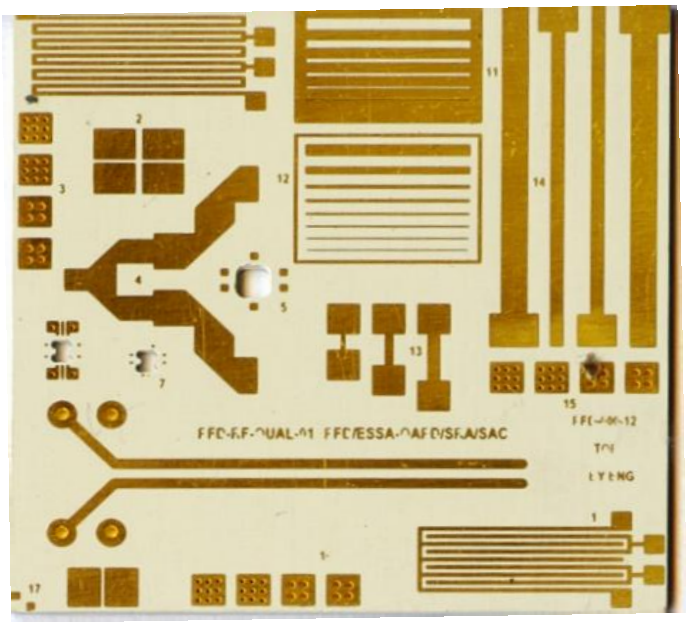
Description	Requirements
Laminate Type	CLTE-XT
Laminate Thickness	20 mil
Basic Copper thickness	½ oz (17 µm)
Type of Finish	Gold finish
Track width / Spacing (min)	0.12 mm
Gold plating Thickness (min)	2 µm (2 to 8 µm)
Hole Size (min)	0.3mm
Gold plating thickness in PTH	2 to 15 µm
Slot size (min)	0.8 x 1.5 mm

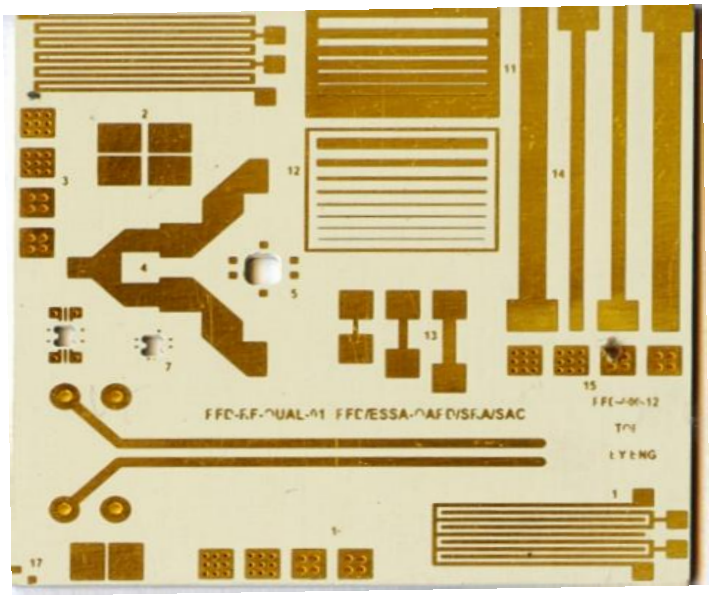
Photograph



<table>
<tr><th colspan="3">45. PTH and Pattern generation with Gold finished PCBs on TMM 6 having laminate thickness 25 mil & ½ Oz basic Copper</th></tr>
<tr><td>Salient Features</td><td colspan="2">Drilling of 25 mil thick TMM 6 laminate with ½ Oz basic Cu is being done on high speed CNC drilling machine followed PTH process and soft gold plating. After image transfer by using a negative photo film, gold and copper etching is carried out under the controlled condition which ensures minimum overhang and 130 micron lines and spacing can be achieved on a total minimum 50 micron copper thickness. Slot making and routing process is being carried out for the required size on CNC drilling machine.</td></tr>
<tr><td>Qualification test plan</td><td colspan="2">SAC/SRA/GEN/PQP/12.0/July 2013, Qualification Test plan for Gold plating / Solder Coating (using HAL) & pattern Generation Process of PCB fabrication with PTH on PTFE laminates.
PID No.: SAC\ESSA\EFMG\PFD\PID\01\JULY, 2015</td></tr>
<tr><td rowspan="10">Qualification Specifications</td><td>Description</td><td>Requirements</td></tr>
<tr><td>Laminate Type</td><td>TMM 6</td></tr>
<tr><td>Laminate Thickness</td><td>25 mil</td></tr>
<tr><td>Basic Copper thickness</td><td>½ oz (17 µm)</td></tr>
<tr><td>Type of Finish</td><td>Gold finish</td></tr>
<tr><td>Track width / Spacing (min)</td><td>0.12 mm</td></tr>
<tr><td>Gold plating Thickness (min)</td><td>2 µm (2 to 8 µm)</td></tr>
<tr><td>Hole Size (min)</td><td>0.3mm</td></tr>
<tr><td>Gold plating thickness in PTH</td><td>2 to 15 µm</td></tr>
<tr><td>Slot size (min)</td><td>0.8 x 1.5 mm</td></tr>
<tr><td>Photograph</td><td colspan="2">  </td></tr>
</table>

<table>
<tr><th colspan="3">46. PTH and Pattern generation with Gold finished PCBs on TMM10i having laminate thickness 15 mil & ½ Oz basic Copper</th></tr>
<tr><td>Salient Features</td><td colspan="2">Drilling of 15 mil thick TMM10i laminate with ½ Oz basic Cu is being done on high speed CNC drilling machine followed PTH process and soft gold plating. After image transfer by using a negative photo film, gold and copper etching is carried out under the controlled condition which ensures minimum overhang and 130 micron lines and spacing can be achieved on a total minimum 50 micron copper thickness. Slot making and routing process is being carried out for the required size on CNC drilling machine.</td></tr>
<tr><td>Qualification test plan</td><td colspan="2">SAC/SRA/GEN/PQP/12.0/July 2013, Qualification Test plan for Gold plating / Solder Coating (using HAL) & pattern Generation Process of PCB fabrication with PTH on PTFE laminates.
PID No.: SAC\ESSA\EFMG\PFD\PID\01\JULY, 2015</td></tr>
<tr><td rowspan="10">Qualification Specifications</td><td>Description</td><td>Requirements</td></tr>
<tr><td>Laminate Type</td><td>TMM10i</td></tr>
<tr><td>Laminate Thickness</td><td>15 mil</td></tr>
<tr><td>Basic Copper thickness</td><td>½ oz (17 µm)</td></tr>
<tr><td>Type of Finish</td><td>Gold finish</td></tr>
<tr><td>Track width / Spacing (min)</td><td>0.12 mm</td></tr>
<tr><td>Gold plating Thickness (min)</td><td>2 µm (2 to 8 µm)</td></tr>
<tr><td>Hole Size (min)</td><td>0.3mm</td></tr>
<tr><td>Gold plating thickness in PTH</td><td>2 to 15 µm</td></tr>
<tr><td>Slot size (min)</td><td>0.8 x 1.5 mm</td></tr>
<tr><td>Photograph</td><td colspan="2">  </td></tr>
</table>

<table>
<tr><th colspan="3">47. NON PTH and Pattern generation with Gold finished PCBs on TMM10i having laminate thickness 50 mil & ½ Oz basic Copper</th></tr>
<tr><td>Salient Features</td><td colspan="2">Drilling of 50 mil thick TMM10i laminate with ½ Oz basic Cu is being done on high speed CNC drilling machine followed by soft gold plating. After image transfer by using a negative photo film, gold and copper etching is carried out under the controlled condition which ensures minimum overhang and 100 micron lines and spacing. Routing process is being carried out for the required size on CNC drilling machine.</td></tr>
<tr><td>Qualification test plan</td><td colspan="2">SAC/SRA/GEN/PQP/12.0/July 2013, Qualification Test plan for Gold plating / Solder Coating (using HAL) & pattern Generation Process of PCB fabrication with PTH on PTFE laminates.
PID No.: SAC\ESSA\EFMG\PFD\PID\01\JULY, 2015</td></tr>
<tr><td rowspan="7">Qualification Specifications</td><td>Description</td><td>Requirements</td></tr>
<tr><td>Laminate Type</td><td>TMM10i</td></tr>
<tr><td>Laminate Thickness</td><td>50 mil</td></tr>
<tr><td>Basic Copper thickness</td><td>½ oz (17 µm)</td></tr>
<tr><td>Type of Finish</td><td>Gold finish</td></tr>
<tr><td>Track width / Spacing (min)</td><td>0.100 mm</td></tr>
<tr><td>Gold plating Thickness (min)</td><td>2 µm (2 to 8 µm)</td></tr>
<tr><td>Photograph</td><td colspan="2">  </td></tr>
</table>

<table>
<tr><th colspan="3">48. NON PTH and Pattern generation with Gold finished PCBs on RT Duroid 6010 having laminate thickness 50 mil & ½ Oz basic Copper</th></tr>
<tr><td>Salient Features</td><td colspan="2">Drilling of 50 mil thick TMM10i laminate with ½ Oz basic Cu is being done on high speed CNC drilling machine followed by soft gold plating. After image transfer by using a negative photo film, gold and copper etching is carried out under the controlled condition which ensures minimum overhang and 100 micron lines and spacing. Routing process is being carried out for the required size on CNC drilling machine.</td></tr>
<tr><td>Qualification test plan</td><td colspan="2">SAC/SRA/GEN/PQP/12.0/July 2013, Qualification Test plan for Gold plating / Solder Coating (using HAL) & pattern Generation Process of PCB fabrication with PTH on PTFE laminates.
PID No.: SAC\ESSA\EFMG\PFD\PID\01\MARCH, 2014</td></tr>
<tr><td rowspan="7">Qualification Specifications</td><td>Description</td><td>Requirements</td></tr>
<tr><td>Laminate Type</td><td>TMM10i</td></tr>
<tr><td>Laminate Thickness</td><td>50 mil</td></tr>
<tr><td>Basic Copper thickness</td><td>½ oz (17 µm)</td></tr>
<tr><td>Type of Finish</td><td>Gold finish</td></tr>
<tr><td>Track width / Spacing (min)</td><td>0.100 mm</td></tr>
<tr><td>Gold plating Thickness (min)</td><td>2 µm (2 to 8 µm)</td></tr>
<tr><td>Photograph</td><td colspan="2">  </td></tr>
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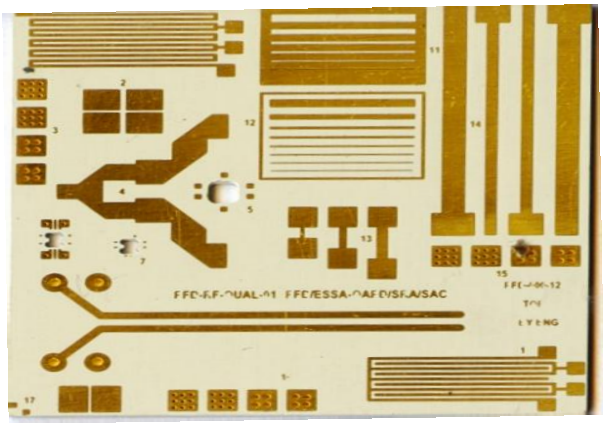
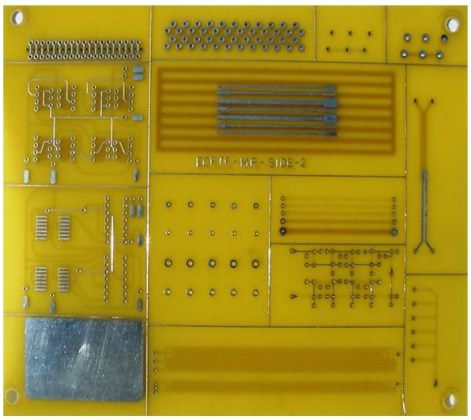
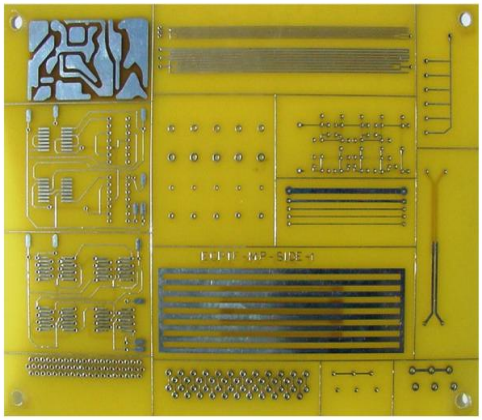
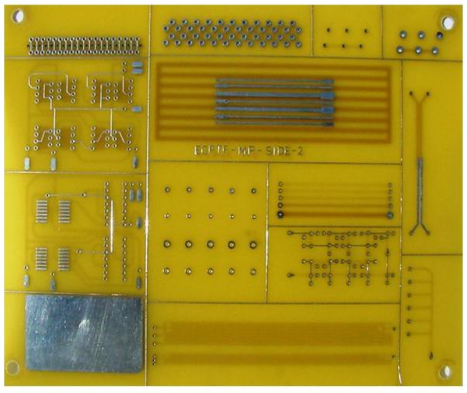
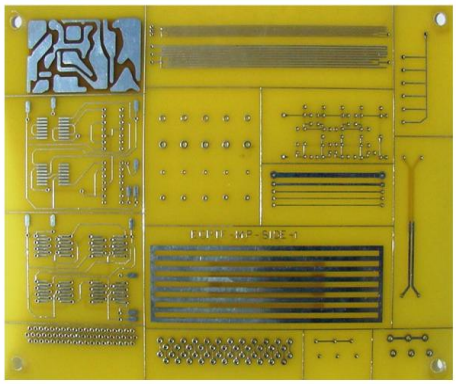
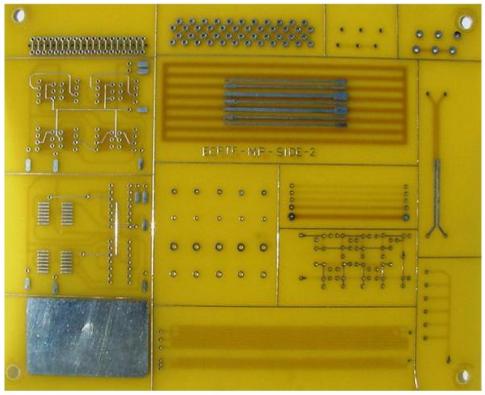
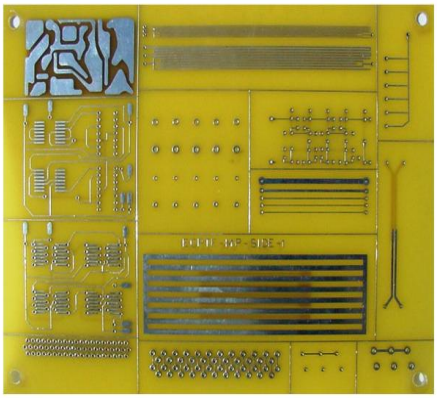
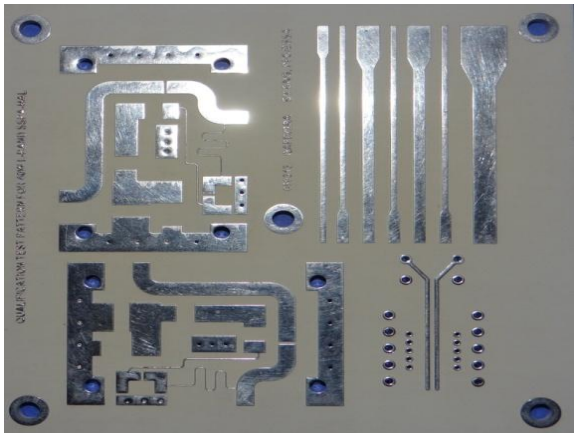
<table>
<tr><th colspan="3">49. NON PTH and Pattern generation with Gold finished PCBs on RT Duroid 5880 having laminate thickness 50 mil & ½ Oz basic Copper</th></tr>
<tr><td>Salient Features</td><td colspan="2">Drilling of 50 mil thick TMM10i laminate with ½ Oz basic Cu is being done on high speed CNC drilling machine followed by soft gold plating. After image transfer by using a negative photo film, gold and copper etching is carried out under the controlled condition which ensures minimum overhang and 100 micron lines and spacing. Routing process is being carried out for the required size on CNC drilling machine</td></tr>
<tr><td>Qualification test plan</td><td colspan="2">SAC/SRA/GEN/PQP/12.0/July 2013, Qualification Test plan for Gold plating / Solder Coating (using HAL) & pattern Generation Process of PCB fabrication with PTH on PTFE laminates.
PID No.: SAC\ESSA\EFMG\PFD\PID\01\MARCH, 2014</td></tr>
<tr><td rowspan="8">Qualification Specifications</td><td>Description</td><td>Requirements</td></tr>
<tr><td>Laminate Type</td><td>RT5880</td></tr>
<tr><td>Laminate Thickness</td><td>0.8mm</td></tr>
<tr><td>Basic Copper thickness</td><td>½ oz (17 µm)</td></tr>
<tr><td>Type of Finish</td><td>Gold finish</td></tr>
<tr><td>Track width / Spacing (min)</td><td>0.250 mm / 0.250 mm</td></tr>
<tr><td>Gold plating Thickness (min)</td><td>2 µm (2 to 8 µm)</td></tr>
<tr><td>Hole Size (min)</td><td>0.3mm / 0.8mm</td></tr>
<tr><td>Photograph</td><td colspan="2">  </td></tr>
</table>

<table>
<tr><th colspan="3">50. DSB PTH and HAL finished PCB on Glass Epoxy FR5 grade (Tg 150 ^{0} C) having laminate thickness 1.6mm & 1 Oz basic Copper</th></tr>
<tr><td>Salient Features</td><td colspan="2">Process is being carried out by electro less copper plating for PTH with pattern up plating process on 1oz thick copper cladded 1.6 mm thick FR5 laminate. Tin plating is used as a etch resist during chemical etching process. Finally hot air leveling process is being done as final board finish. PTH and NPTH hole drilling and routing process are carried out on high speed CNC drilling machine.</td></tr>
<tr><td>Qualification test plan</td><td colspan="2">ISRO-PAX-302, Issue-1, “Test specification for printed circuit boards”. PID No.: SAC\ESSA\EFMG\PFD\PID PFD/PID\04 REV 0\2013 APRIL 2013</td></tr>
<tr><td rowspan="7">Qualification Specifications</td><td>Description</td><td>Requirements</td></tr>
<tr><td>Laminate Type</td><td>FR5 (Poly-functional grade) , 1 oz each side, as per IPC-4101/23</td></tr>
<tr><td>Laminate Thickness</td><td>1.6mm</td></tr>
<tr><td>Basic Copper thickness</td><td>1oz (35 µm)</td></tr>
<tr><td>Type of Finish</td><td>HAL Solder finish (4 to 30 µm)</td></tr>
<tr><td>Track width / Spacing (min)</td><td>0.250 mm</td></tr>
<tr><td>Hole Size (min)</td><td>0.5mm</td></tr>
<tr><td>Photograph</td><td colspan="2"> 
Side -2
 
Side - 1</td></tr>
</table>

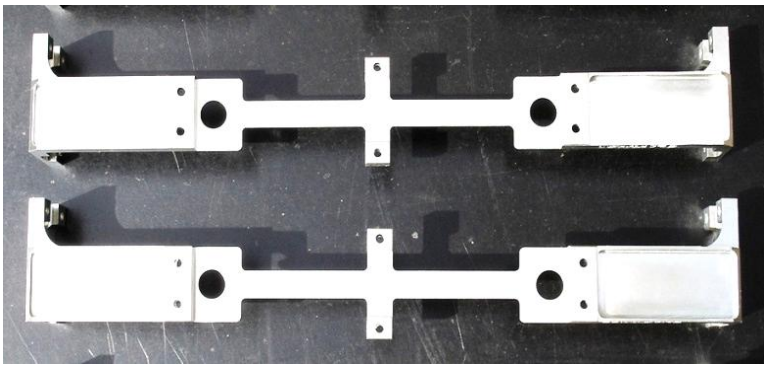
<table>
<tr><th colspan="3">51. DSB PTH and HAL finished PCB on High Tg (175^{0}C) Multifunctional Laminates having laminate thickness 0.8mm & 1 Oz basic Copper</th></tr>
<tr><td>Salient Features</td><td colspan="2">Process is being carried out by electro less copper plating for PTH with pattern up plating process on 1oz thick copper clad High Tg (175^{0}C) Multifunctional Laminates. To make the hole wall receptive to PTH process, desmaring process is being done. The Tin plating is used as a etch resist during chemical etching process. Hot air solder leveling process is being done to provide solderable finish. Drilling and routing is carried out on high speed CNC drilling machine.</td></tr>
<tr><td>Qualification test plan</td><td colspan="2">ISRO-PAX-302, Issue-1, “Test specification for printed circuit boards”.
PID No.: SAC\ESSA\EFMG\PFD\PID\05\ REV 0 \ 2013 MAY 2013</td></tr>
<tr><td rowspan="7">Qualification Specifications</td><td>Description</td><td>Requirements</td></tr>
<tr><td>Laminate Type</td><td>Glass epoxy laminate, 1 oz each side, as per IPC-4101, Nelco N4000-6 laminate</td></tr>
<tr><td>Laminate Thickness</td><td>0.8mm</td></tr>
<tr><td>Basic Copper thickness</td><td>1oz (35 µm)</td></tr>
<tr><td>Type of Finish</td><td>HAL Solder finish (4 to 30 µm)</td></tr>
<tr><td>Track width / Spacing (min)</td><td>0.250 mm</td></tr>
<tr><td>Hole Size (min)</td><td>0.5 mm</td></tr>
<tr><td>Photograph</td><td colspan="2"> 
Side -2
 
Side - 1</td></tr>
</table>

<table>
<tr><th colspan="3">52. DSB PTH and HAL finished PCB on High Tg (175^{0}C) Multifunctional Laminates having laminate thickness 2.4mm & 2 Oz basic Copper</th></tr>
<tr><td>Salient Features</td><td colspan="2">Process is being carried out by electro less copper plating for PTH with pattern up plating process on 2 oz thick copper clad High Tg (175^{0}C) Multifunctional Laminates. To make the hole wall receptive to PTH process, desmaring process is being done. The Tin/Solder plating is used as a etch resist during chemical etching process. Hot air solder leveling process is being done to provide solderable finish. Drilling and routing is carried out on high speed CNC drilling machine.</td></tr>
<tr><td>Qualification test plan</td><td colspan="2">ISRO-PAX-302, Issue-1 “Test specification for printed circuit boards”. PID No.: SAC\ESSA\EFMG\PFD\PID\05\ REV 0 \ 2013 MAY 2013</td></tr>
<tr><td rowspan="7">Qualification Specifications</td><td>Description</td><td>Requirements</td></tr>
<tr><td>Laminate Type</td><td>Glass epoxy laminate, 1 oz each side, as per IPC-4101, Nelco N4000-6 laminate</td></tr>
<tr><td>Laminate Thickness</td><td>2.4 mm</td></tr>
<tr><td>Basic Copper thickness</td><td>2oz (70 µm)</td></tr>
<tr><td>Type of Finish</td><td>HAL Solder finish (4 to 30 µm)</td></tr>
<tr><td>Track width / Spacing (min)</td><td>0.250 mm</td></tr>
<tr><td>Hole Size (min)</td><td>0.5mm</td></tr>
<tr><td>Photograph</td><td colspan="2"> 
Side -2
 
Side - 1</td></tr>
</table>

<table>
<tr><th colspan="3">53. DSB PTH and HAL finished PCB on TMM10i having laminate thickness 100mil & 2 Oz basic Copper</th></tr>
<tr><td>Salient Features</td><td colspan="2">Process is being carried out by electro less copper plating for PTH with pattern up plating process on 2 oz thick copper clad TMM10i. The Tin/Solder plating is used as a etch resist during chemical etching process. Hot air solder leveling process is being done to provide solderable finish. Drilling and routing is carried out on high speed CNC drilling machine.</td></tr>
<tr><td>Qualification test plan</td><td colspan="2">SAC/SRA/GEN/PQP/12.0/July 2013, Qualification Test plan for Gold plating / Solder Coating (using HAL) & pattern Generation Process of PCB fabrication with PTH on PTFE laminates.
PID No.: PCB/PFD/ 01/ DEC.- 2010</td></tr>
<tr><td rowspan="8">Qualification Specifications</td><td>Description</td><td>Requirements</td></tr>
<tr><td>Laminate Type</td><td>TMM10i</td></tr>
<tr><td>Laminate Thickness</td><td>100 mil</td></tr>
<tr><td>Basic Copper thickness</td><td>2 oz (70 µm)</td></tr>
<tr><td>Type of Finish</td><td>HAL solder leveling finish</td></tr>
<tr><td>Track width / Spacing (min)</td><td>0.100 mm</td></tr>
<tr><td>HAL solder leveling thickness (min)</td><td>4 to 30 µm</td></tr>
<tr><td>Hole Size (min)</td><td>0.5 mm</td></tr>
<tr><td>Photograph</td><td colspan="2">  </td></tr>
</table>

54. Electroless Nickel Immersion Gold on Semi-Rigid Cables for Space Use

Salient Features	Electro-less Nickel Immersion Gold plating is being done on the semi - rigid cable to protect copper from environment and to provide the good solderable, less susceptible to whisker coating than conventional tin plating.	
Qualification test plan	**PID:** PCB -2 REV 1/PFD/APRIL 2012	
Qualification Specifications	**Description**	**Requirements**
	Semirigid Cable	Bare copper finish semi-rigid cable.
	Semirigid Cable Size	0.085” and 0.141” dia cable
	Type of Finish	ENIG gold finish
	Nickel plating Thickness	8-12µ
	Immersion gold plating Thickness	<0.1 µ
Photograph		

<table>
<tr><th colspan="3">55. Tin plating on Copper Braid assembly</th></tr>
<tr><td>Salient Features</td><td colspan="2">Cold fingers and copper braid assembly made from copper are required for better thermal conductivity for the IRS, CARTOSAT and RESOURCESAT series satellites. These copper components require tin plating mainly for solderability and corrosion resistance point view.</td></tr>
<tr><td>Qualification test plan</td><td colspan="2">PID: PCB / ECPTF / AUGUST 09</td></tr>
<tr><td rowspan="4">Qualification Specifications</td><td>Description</td><td>Requirements</td></tr>
<tr><td>Copper braid</td><td>Bare copper finish</td></tr>
<tr><td>Type of Finish</td><td>Tin finish on braid assembly</td></tr>
<tr><td>Tin plating</td><td>>12 microns</td></tr>
<tr><td>Photograph</td><td colspan="2">  </td></tr>
</table>

<table>
<tr><th colspan="3">56. Helical antenna strip making from 2mil thick Kapton material with 1Oz Cu</th></tr>
<tr><td>Salient Features</td><td colspan="2">Helical antenna strip having length 1200 mm and width 4 mm are generated on high speed CNC drilling machine from thin copper clad Kapton Flexible laminate. Pattern geometry shall be maintained constant throughout the length of strip and edges shall be free from burr.</td></tr>
<tr><td>Qualification test plan</td><td colspan="2">-</td></tr>
<tr><td rowspan="5">Qualification Specifications</td><td>Description</td><td>Requirements</td></tr>
<tr><td>Laminate Type</td><td>2 mil thick Kapton laminate</td></tr>
<tr><td>Laminate length & width</td><td>1200 mm (typ.) 4 mm (typ.)</td></tr>
<tr><td>Basic Copper thickness</td><td>35 micron</td></tr>
<tr><td>Type of Finish</td><td>Bare copper, no additional finish</td></tr>
<tr><td>Photograph</td><td colspan="2"> 
  </td></tr>
</table>

57. Vacuum deposition of Paraxylene (Parylene Conformal Coating Process) for Spaceborne PCB assemblies

Salient Features

The coating deposition process involves vaporisation, payrolysis & sublimation of Parylene-C dimer from granules to uniform non conductive protective coating of 12-20 micron on wired PCB assemblies. It meets the requirements of MIL-I-46058 and has very low out-gassing properties. This process protects the wired PCBs from humidity, salts related effects which might stress the wired components/PCB during storage, transit.

Parameter	Specification
Deposition Rate	5 Micron/Hr (Parylene C) 1 Micron/Hr (Parylene N)
Max PCB Size	200x 175mm
Card Batch	5 PCBs of Maximum Size

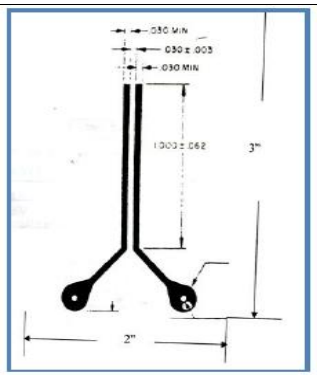
Qualification test plan

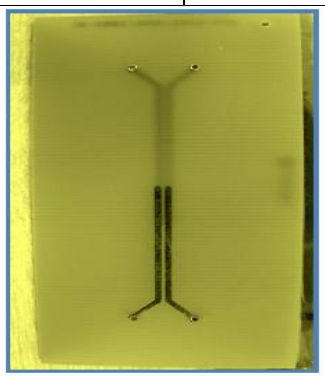
PID: SAC/ESSG/PFF -01-04

Major Specifications of Qualified Process

Parameter	Specification
Coating Material	Parylene C , Parylene N in Powder form
Coating Thickness	15-25 Micron
Insulation Resistance(Ω)	1.5 Terra Ohm min.
Dielectric Withstand Voltage (DWV)	1500 V- 1min

Photograph





58. PCB Assemblies Comprising Of Through Hole & Fine Pitch Surface Mount Devices

Salient Features

Manual Soldering assembly of Mixed technology components described as below:

Parameter	Specification
Component Type	Leaded & SMD
Component Style	Resistor, Capacitor, DIP, Flat Pack, CQFP, D Sub/SMA Connectors
Pitch	Up to 16 Mil
Lead thickness	0.12 mm for CQFP & 0.3 mm Lead dia for PTH components
Maximum lead count	352 for fine pitch

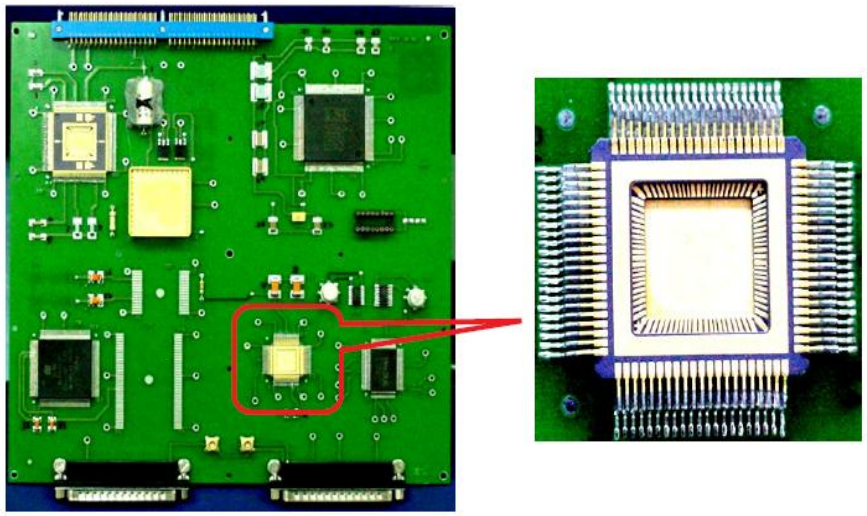
Qualification test plan

SAC\SRG\QPS-QAED\TR\23\2006
PID: SAC/ESSG/PFF/SMT/12/2005, Rev01

Major Specifications of Qualified Process

Parameter	Specification	Achieved
Pull Strength –CQFP	0.5 kgf	0.75-1.2 kgf
Shear strength SMD	2.5 kgf	4 to 17.5 kgf
Pull Strength	5 kgf	6-8 kgf

Photograph



59. Parylene Conformal Coating on SMOBC PCB

Salient Features

The coating deposition process involves vaporisation, payrolysis & sublimation of Parylene-C dimer from granules to uniform non conductive protective coating of 12-20 micron on wired PCB assemblies. It meets the requirements of MIL-I-46058 and has very low out-gassing properties. This process protects the wired PCBs from humidity, salts, and ESD related effects which might stress the wired components/PCB during storage, transit.

Parameter	Specification
Deposition Rate	5 Micron/Hr (Parylene C) 1 Micron/Hr (Parylene N)
PCB Masking	Solder Mask over bare copper

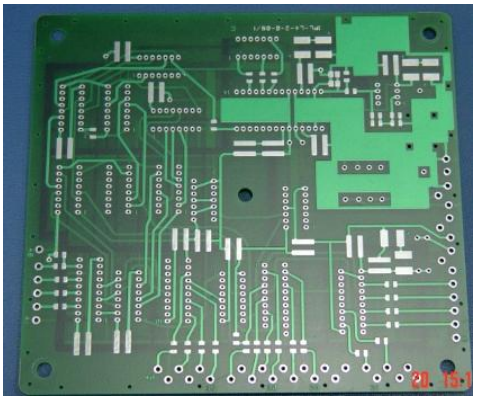
Qualification test plan

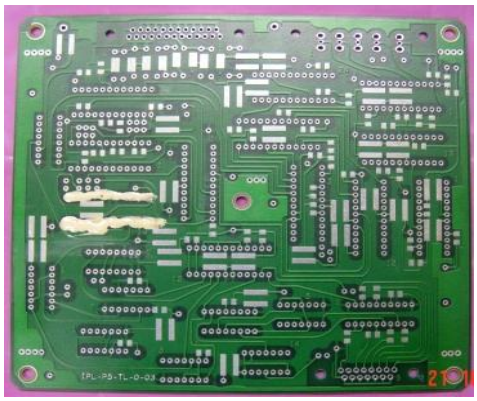
SAC/QAED-SRG/QPS/TR/01/2006
PID: SAC/ESSG/PFF -01-04

Major Specifications of Qualified Process

Parameter	Specification
Coating Material	Parylene C , Parylene N in Powder form
Coating Thickness	15-25 Micron
Insulation Resistance(Ω)	1.5 Terra Ohm min.
Dielectric Withstand Voltage (DWV)	1500 V- 1min
PCB Size	300x300 mm

Photograph





60. Lead Forming, Mounting/Manual Soldering & Dam Formation (Device Encapsulation) using RTV DC 93-500 For CQFP / Flat Pack

Salient Features

Process	Device Type	Lead thickness	Lead Count	Pitch
Lead Forming, Mounting / Manual Soldering	CQFP, FP	0.12-0.25 mm	8-352	Up to 16 Mil
Dam Formation (Device Encapsulation)	CQFP	0.12 mm	100 or more	20 Mil or less

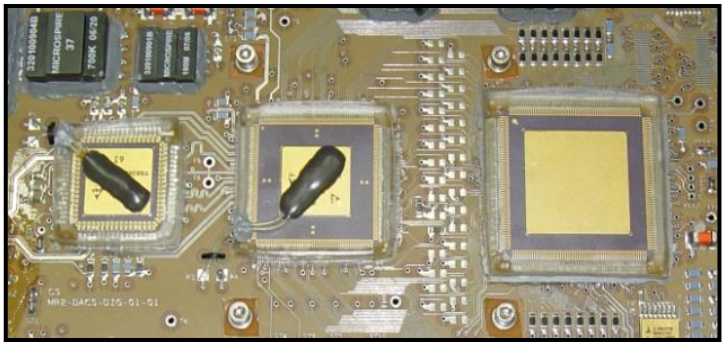
Qualification test plan

PID: SAC/ESSG/PFF/01/05

Major Specifications of Qualified Process

Test	Specification	Achieved Results
Pull Test-Fine Pitch CQFP/FPs	0.5 Kgf	0.75-1.2 Kgf

Photograph



61. Micro D Connector (Solderable) Assembly with Polyamide Shielded Cables for TWSAT

Salient Features

Micro-D sub-miniature connectors offer significant reduction in size & weight, with excellent reliability. Available Pre-fabricated harness assemblies use wires crimped to the contacts which are permanently fixed in the shell with epoxy. However, with pre-crimped harness assemblies, flexibility for modifications in harness routing, changes in configuration and repair are severely restricted. The indigenous process development & qualification enables the effective utilisation of solderable cup micro d connector with desired configuration with a facility of modification at any stage. Micro Ds are comparatively lesser in weight (60%) & volume (40%) with respect to Normal D Sub for same pin count.

Connector	Pin/Plug Pitch	Wire gauge	Maximum Pin/Plug Count
Micro D	1.27 mm	26 & 28 AWG	37

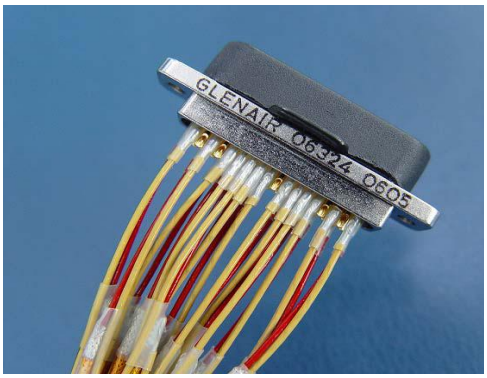
Qualification test plan

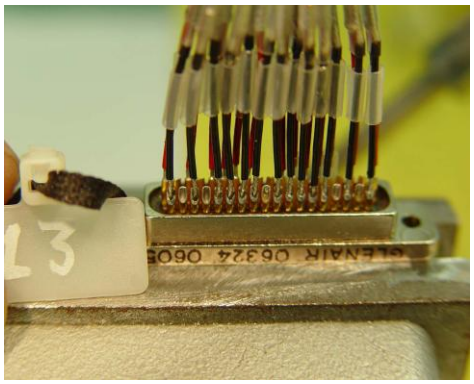
QPS-QAED/2007/45
PID: SAC/ESSG/EFTF/PFF –01 MAY- 2007

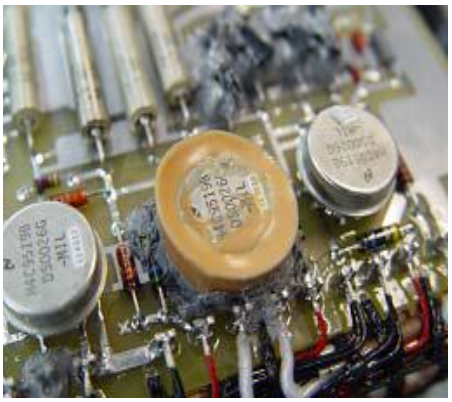
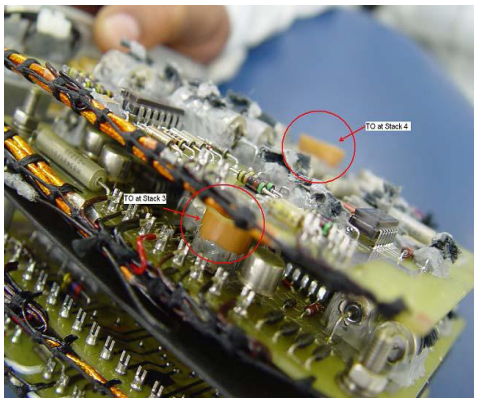
Major Specifications of Qualified Process

Specification	Requirement (Mil-DTL-83513)	Achieved
Contact Resistance	32 mΩ Max	5.7- 6.8 mΩ
Wire Pull Strength	2.2 Kgf	2.7-7 Kgf

Photograph





62. Thermally Conductive H-74 Epoxy Application on TO Can IC's in OCM payloads of OS-II	
Salient Features	Global Area Coverage (GAC) by OCM-II P/L to meet the demand from the users across the globe has necessitated increasing payload 'ON' period (from 12 to 40 minutes) for several consecutive orbits thus reducing the 'Cool Off' period to 60 minutes before scanning the next orbit. Under Such conditions thermal team has estimated the ambient temperature of payload to rise to 42°C, which poses the risk of certain TO can devices to reach at the junction temperature. For adequate heat dissipation, the process is developed, qualified & successfully utilised in OCM-II payload.
Qualification test plan	Eval. Report -29/10/2007 Annex-B **PID**: SACESSGEFTFPFF –01-Nov- 2007
Major Specifications of Qualified Process	Process is adequate in thermal dissipation in active devices by 20-30 deg C depending upon the configuration.
Photograph	 

63. Assembly Of "Huber Suhner" SMA Solderable Connectors (11 SMA 50-3-15) On MF-141 Coaxial Cable

Salient Features

Huber Suhner make MULTIFLEX microwave cables are the flexible alternative to SEMI RIGID cables. They are used in commercial and military RF and microwave airborne systems, communications systems, satellite ground stations.

Cable Type	Cable Diameter	Frequency of Operation
Multi Flex-141	0.141 Inch	Up to 18 Ghz

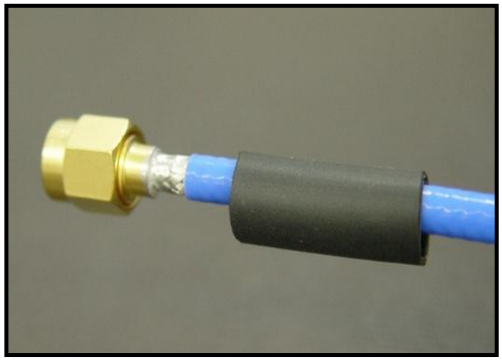
Qualification test plan

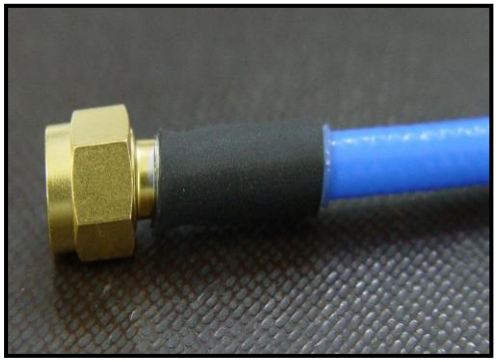
PID: SAC/ESSG/EFTF/EFF/PID/O1

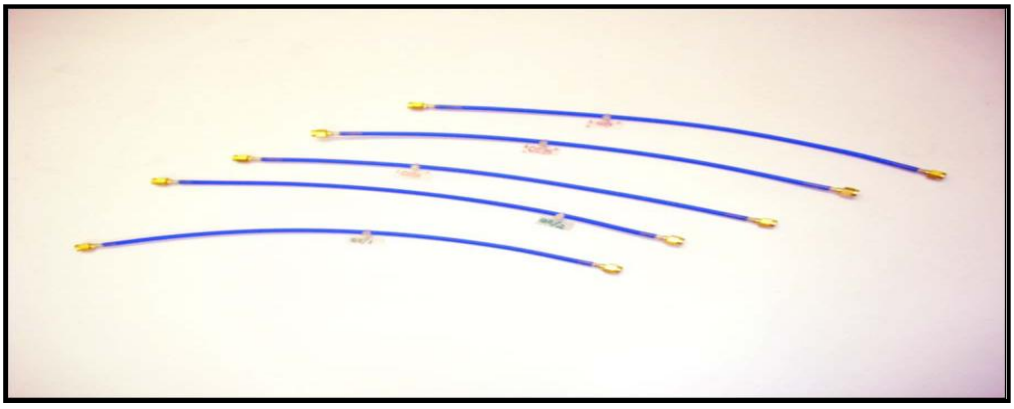
Major Specifications of Qualified Process

Connector Type	Interconnection Process
SMA Solderable Connectors (11 SMA 50-3-15)	Soldering

Photograph





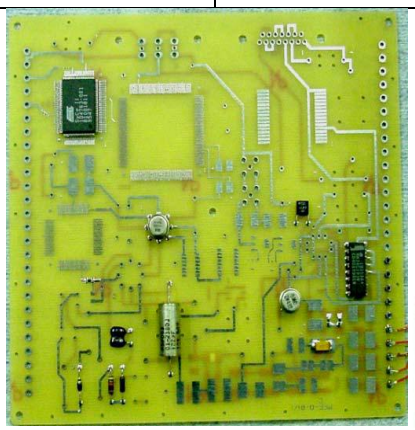


64. Vapour Phase Parylene Conformal Coating of PCB Assemblies utilising PDS 2060 PC System

Salient Features	**Parameter**	**Specification**
	Coating Material	Parylene C, Parylene N in Powder form
	Coating Thickness	15-25 Micron
	Deposition Rate	5 Micron/Hr (Parylene C) 1 Micron/Hr (Parylene N)
	PCB Size	300x300 mm
	Card Batch	10 PCBs of Maximum Size
Qualification test plan	SAC/SRG/QPS-QAED/TR/17/2009 **PID:** SACESSGEFTFPFF -20-June-2009	

Major Specifications of Qualified Process	**Parameter**	**Specification**	**Achieved**
	Insulation Resistance(Ω)	1.5 Terra Ohm min.	1.7-6 Terra Ohm
	Dielectric Withstand Voltage (DWV)	1500 V- 1min	1500 V- 1min No evidence of flashover, arching or de-lamination was found during the test. All the test samples meet the requirements

Photograph



65. Crimpable Micro D Connector Harness Assembly process

Salient Features

In new package design of advance projects, use of Micro D connectors are essential as a step towards miniaturizations & weight saving. Crimpable Micro-D Connectors are having inherited advantage of small foot print due to its miniature size and les weight as compared to Normal D sub Connectors. In TWSAT, Solderable Cup Micro d Connectors was qualified and implemented and as an upgradatation, crimp version of Micro-D Connectors have also successfully taken up for harness & assembly qualification.

Connector	Pin/ Plug Pitch	Wire gauge	Wire Type	Maximum Pin/Plug Count
Micro D	1.27 mm	26/28 AWG	Polyamide, Spec-55, LVDS, Polyamide Shielded cables, RG-316, TP	37

Qualification test plan

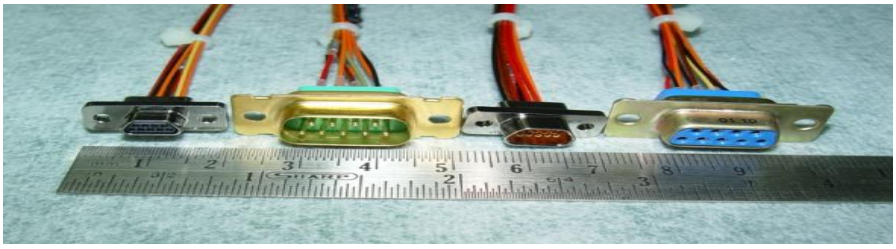
QPS-QAED/2010/79
PID: SACESSAEFTFPFF H Crimp -10-01

Major Specifications of Qualified Process

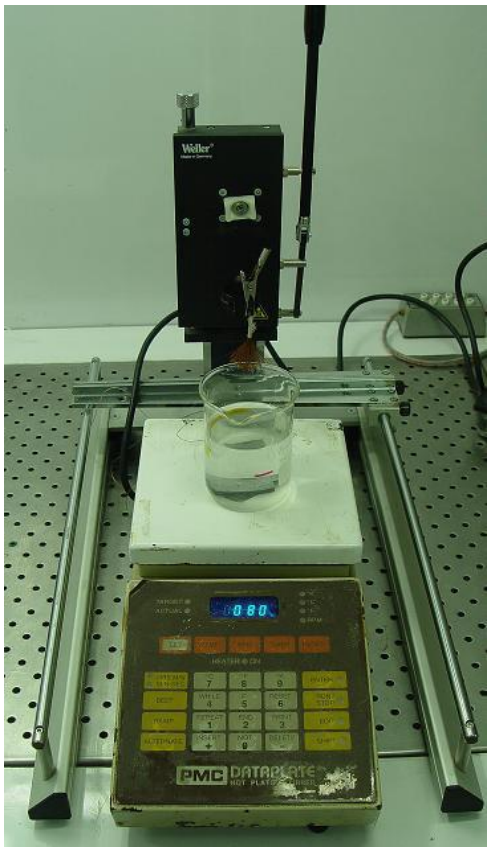
Specification	Requirement (Mil-DTL-83513)	Achieved
Contact Resistance	32 mΩ Max	8 mΩ
Wire Pull Strength	30N (28AWG wire) 45N (26AWG wire)	35-40 N(28AWG wire) 55-70 N(26AWG wire)

Photograph

Cross section of crimped joint



66. Multistrand Enamelled Copper wire (Litz) Insulation removal & Tinning

Salient Features	In new package design of High power electronic power conditioner for 100 W solid state power amplifiers (GSAT-7), coils made of Multistrand enamelled copper wires is to utilized due to their high current carrying capacity. Enamel removal of these coils requires specialized procedure which ensures the full insulation removal from each individual wire thread which is very essential for optimum performance of the coil	
Qualification test plan	Eval Report-06/02/08 **PID:** SACESSAEFTFPFF S TINNING -11-01	
Major Specifications of Qualified Process	**Process**	**Method**
	Insulation Removal	Chemical Insulation removal (40% W/V NaOH Solution)
	Tinning	Solder dip(Sn60/Pb40)
Photograph		 Wire Bunch after insulation removal 

<table>
<tr><th colspan="3">67. Realisation of Ortho-Mode Transducer with solder as a Metal Joinery process for MM wave Sounder</th></tr>
<tr><td>Salient Features</td><td colspan="2">Soldering activities are considered to be the prime assembly mechanism for electronic components wiring on printed circuit boards. Use of Solder joint exclusively for mechanical, structural application is rare as mechanical structures are designed to endure greater magnitude of thermal and vibration loads compared to electronic packages. Soldering as a mechanical joining method was developed & qualified to realise the complex OMT feeds.</td></tr>
<tr><td>Qualification test plan</td><td colspan="2">PQ/SOLDERING/03
PID: SAC/SRA/QAMD/TR/00/APRIL-2011</td></tr>
<tr><td rowspan="3">Major Specifications of Qualified Process</td><td>Name of Test</td><td>Results</td></tr>
<tr><td>Tensile test</td><td>100 N/mm^2</td></tr>
<tr><td>Shear test</td><td>30 N/mm^2</td></tr>
<tr><td>Photograph</td><td colspan="2">   </td></tr>
</table>

68. Assembly of Ball Grid Array (BGA) on Space hardware with Hot Gas Reflow

Salient Features

Advance electronic packages demand miniaturization of components with higher pin counts, & convergence of functionalities with robustness. In order to accommodate the increasing number of I/Os needed, the peripheral QFP technology is forced to an ever finer lead pitch with thinner and more fragile leads. The BGAs, taking advantage of the area under the package for the solder sphere interconnections, satisfies the more number of I/O demand using a far coarser pitch. BGAs offer approximately 50% increased silicon density and 60% effective size reduction as compared to QFP devices.

Balls	Ball dia	Pitch	Solder Material
1148	0.65 mm	40 mil	Sn63Pb37

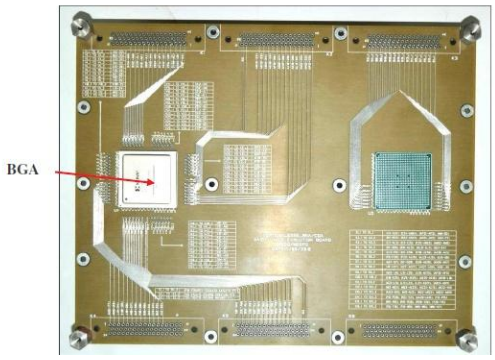
Qualification test plan

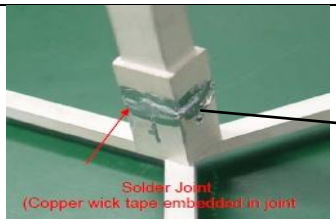
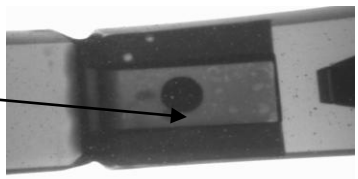
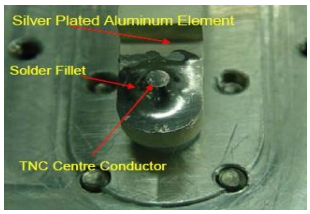
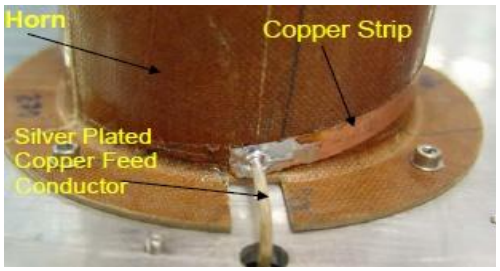
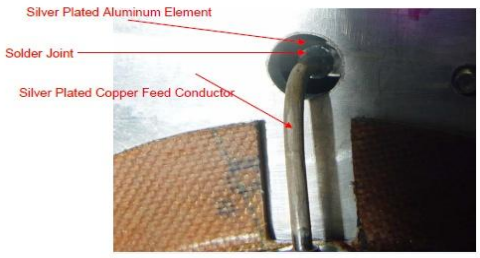
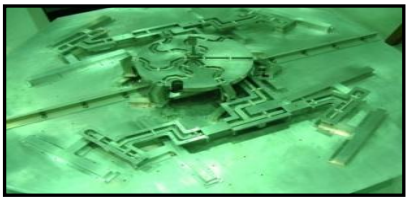
SRA/QAPD-QAEG/2011/80
PID: SACESSAEFMGPEFDSREFLOW-10-03

Major Specifications of Qualified Process

The BGA soldering process using Hot Air Reflow System (ONYX-29) with following configuration can be declared as qualified for field life of 4.3 years in LEO orbit with field operation temperature 0ºC to +40ºC.

Photograph



69. Solder as a Metal Joinery process for S & L5 Band Helical Antenna feed soldering for IRNSS series	
Salient Features	Process development includes soldering of mechanical antenna parts for flexibility and better return loss (-22db) performance. Elements are high thermal dissipative metal parts and process was developed to compensate the heat losses during soldering. Feed was also modified to self align itself prior to soldering.
Qualification test plan	SRA/QAPD-QAEG/2012/23 **PID:** SACESSAEFMGPEFD SOL-HELIX-12-04
Major Specifications of Qualified Process	Solder as metal joinery media has been successfully utilized & qualified for following four types of configuration: ➢ Soldering of two Silver Plated Aluminum Elements ➢ Soldering Activity of Silver plated aluminum element with silver plated copper feed wire ➢ Soldering of gold plated TNC connector with silver plated aluminum element ➢ Soldering of Silver plated copper feed wire with copper strip on horn
Photograph	   8x8 mm Square Al-Interface   Copper Strip of 4 mm & 70 micron Thickness 

70. Ceramic Column Grid Array (CCGA) Assembly & Soldering process development with Hot Gas Reflow

Salient Features

CCGA components are latest packaging in the family of Area Array Devices & similar with BGA in terms of interconnection density & area, however differs in interconnection length & weight. As compared to BGAs, CCGAs are less susceptible to CTE mismatch related failures which is a prominent failure mode for BGAs, thus providing reliability by component design itself. CCGAs also offer ease of processing like cleaning/inspection of outer rows & few inner rows due to the increased gap between device body & PCB surface.

CCGA Device Characteristics	
Device Size	35x35 mm
Device Material	Multilayer Ceramic(CTE~ 6-8 ppm/°c)
Substrate thickness	3 mm
Device Weight	~23 grams
Column Material	90Pb10Sn
Column attach	CLASP (Pd Doped Sn63/Pb37)
Column dia	~0.52mm
Column pitch	1mm
Column Height	2.21 mm

Qualification test plan

SRA/QAPD-QAEG/2012/49

PID: SAC/ESSA/EFMG/PEFD/S/REFLOW-12-01

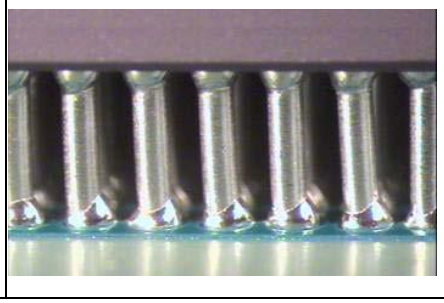
Major Specifications of Qualified Process

The CCGA assemblies have successfully passed the accelerated thermal cycling test and no failure was observed even after 1200 cycles due to solder-joint. This is equivalent to

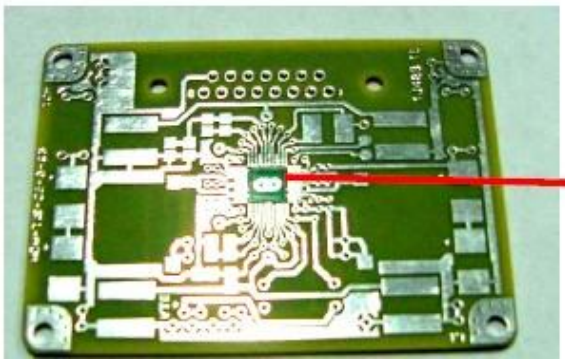
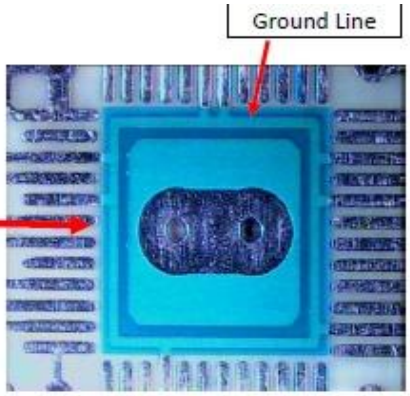
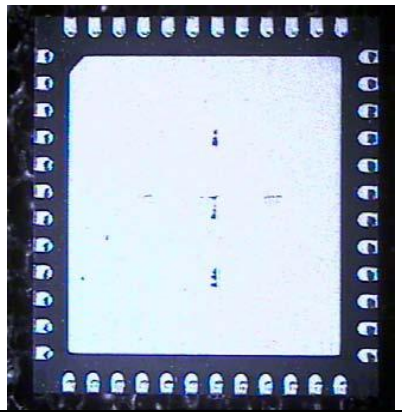
Test Condition	Field Environment	Estimated life
-55°C to +105°C with ramp rate of 3°C/minute	LEO Orbit with 90 minutes cycle, Operating temp. 0°C to +40°C	7 Years
	GEO Orbit with 24 hrs cycle, Operating temp 0°C to +40°C	45 Years

Reliability figure for CCGA joint is calculated to be 0.99974237.

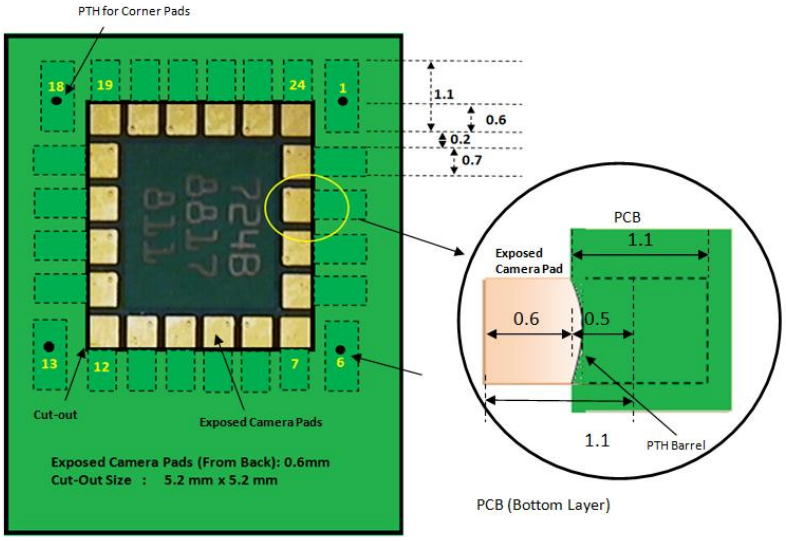
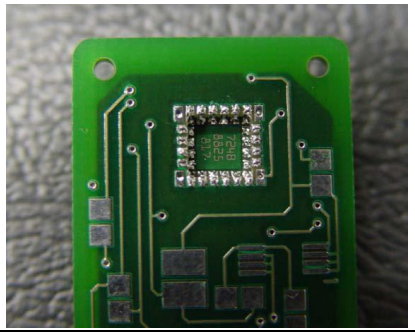
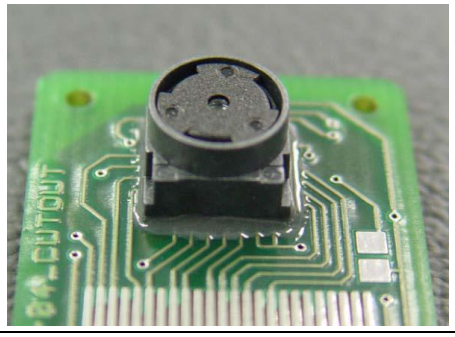
Photograph



71. Quad Flat Pack No Lead (QFN) Assembly & Soldering by Hot Gas Reflow for Mars Orbiter Mission

Salient Features	QFN (MAX1978/MAX1979) packages are planned to be used in temperature controller circuits in TIS payload for MARS mission. QFN (Quad Flat Pack with No Lead) packaging has no leads in sides and essentially has a large thermal pad (Ground Lug) in the centre. These are plastic packages with bottom termination and are being used for the first time in space payload. Soldering & assembly process has been successfully developed & qualified for Flight model subsystems.	
Qualification test plan	SRA/QAEG-QAPD/2013/17 **PID:** SACESSAEFMGPEFDSS201302	
Major Specifications of Qualified Process	**Parameter**	**Specification**
	Pitch	20 Mil
	Pads	49
Photograph	  	

72. Micro Camera Assembly process for Chandrayaan-II Rover

Salient Features	For Chadrayaan-II landing rover configuration requires miniature camera module for imaging purposes. The realization of the flight hardware requires assembly & soldering of Plastic Body Camera Module on the Multi Layer PCB. As the camera body is made of the plastic material, and the lead pattern is of QFN types (without leads) conventional reflow option is not feasible considering degradation of the camera body itself. A novel method was developed which incorporates cutting a window (analogous in size with camera pad layout) on the PCB while making connection through the half open PTH barrels with the help of fine leads (CQFP leads)
Qualification test plan	SRA/QAEG-QAPD/2013/12 **PID:** SACESSAEFMGPEFDS2013-1
Major Specifications of Qualified Process	**Camera Specifications** 
Photograph	 

73. Lid-Sealing Process of Hermetic Package (GMR-A3253) for MMIC, using Hot Gas Reflow Soldering (ONYX 29)

Salient Features

Packaging of bare MMIC die was required to be carried out for the on-going activity of GEOSAT Programme. The requirement generated due to delay in the delivery of FM packaged MMIC mixer devices from M/s OMMIC. It was decided to develop in-house lid-sealing process to realize packaged devices with available FM MMIC die by improvising the existing hot gas reflow soldering system.

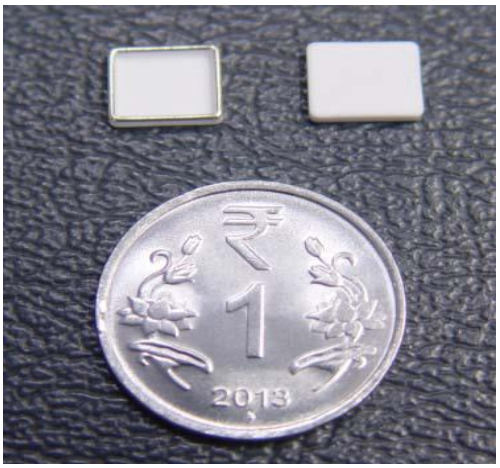
Qualification test plan

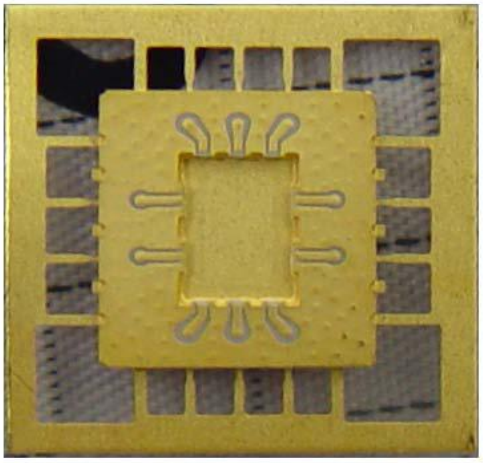
SAC/SRA/GEN/PQR/8.0/May,2015
PID: SAC/ESSA/EFMG/PEFD/S/2013/03

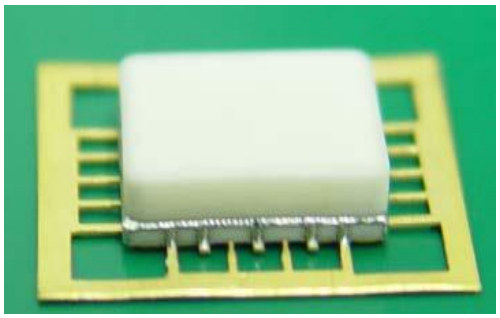
Major Specifications of Qualified Process

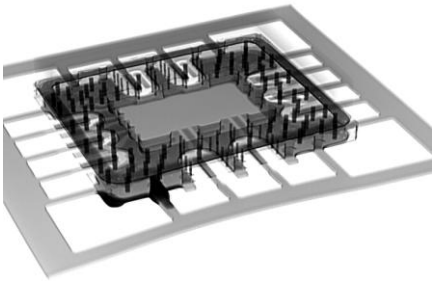
Parameter	Specification	Achieved
Fine Leak	< 5 x 10-8 atm. cc/sec He	1.5- 4 x 10-8 atm. cc/sec He
Gross leak	Nil leak	Nil leak

Photograph









74. Reflow Soldering of Ceramic Column Grid Array (CCGA) with LASER

Salient Features

CCGA components are latest packaging in the family of Area Array Devices & similar with BGA in terms of interconnection density & area, however differs in interconnection length & weight. As compared to BGAs, CCGAs are less susceptible to CTE mismatch related failures which is a prominent failure mode for BGAs, thus providing reliability by component design itself. CCGAs also offer ease of processing like cleaning/inspection of outer rows & few inner rows due to the increased gap between device body & PCB surface.

CCGA Device Characteristics

Device Size	35x35 mm
Device Material	Multilayer Ceramic(CTE~ 6-8 ppm/°c)
Substrate thickness	3 mm
Device Weight	~23 grams
Column Material	90Pb10Sn
Column attach	CLASP (Pd Doped Sn63/Pb37)
Column dia	~0.52mm
Column pitch	1mm
Column Height	2.21 mm

Qualification test plan

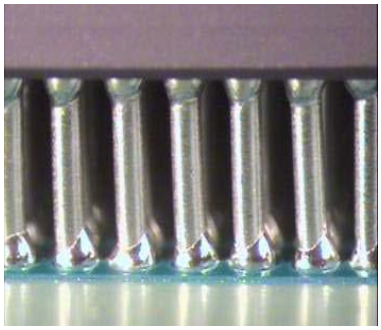
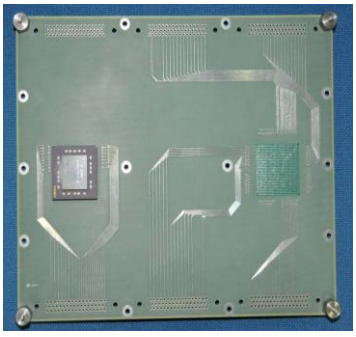
Eval. Report12/06/2015

PID: SAC/ESSA/EFMG/PEFD/LASER-S/06/2015

Major Specifications of Qualified Process

The CCGA assemblies have successfully passed the accelerated thermal cycling test and no failure was observed even after 1200 cycles due to solder-joint. Qualification report is awaited.

Photograph


75. Conformal Coating Removal using Micro Blasting System

Salient Features

Any rework or component replacement or incorporation of jumper wires, etc. is cumbersome on a conformably coated PCB, as this requires special skills and a controlled localized removal of the conformal coating (CC). However, even with utmost care, manual removal of CC may leave physical damage like scratches & cuts on the PCB laminate /conductor. The non-contact CC removal process, using the "Swam-Blaster" system, helps prevent this damage and gives uniform removal as well. Swam-Blaster (Crystal Mark Inc. make) is a machine that provides controlled CC removal The swam-blaster machine has two controls for quantity of powder and for air pressure, such that there desired combination of powder-quantity and air-pressure can be optimized. The powder is not soluble in IPA and cleaned away by this cleaning agent.

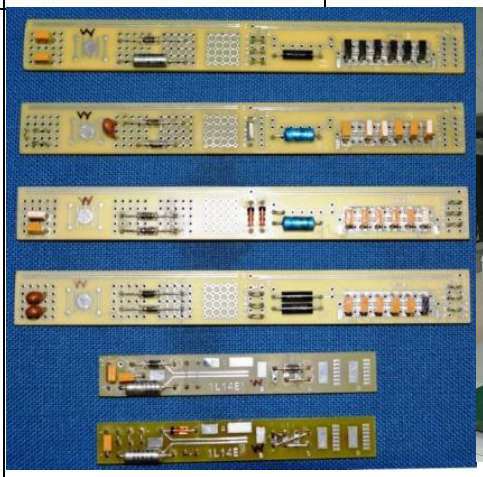
Qualification test plan

SAC/SRA/PEFD/10/May,2015
PID: SAC/ESSA/EFMG/PEFD/LASER-S/04/2015

Major Specifications of Qualified Process

Coating Type for removal	Thickness for removal	
	Requirement	Max Thickness which can be removed
Parylene C	25 Micron	Tested up to 150 microns
Polyurathene	50 Microns	Tested up to 150 microns
Silver Epoxy	100 Microns	Tested up to 150 microns

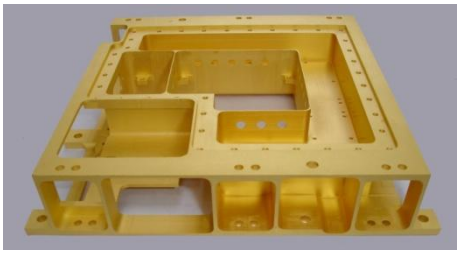
Photograph



76. Gold Plating on Aluminum Alloy 6061	
Process UID No	**STPD / ST - 01**
Brief Description	Developed and qualified the process of Gold Plating on Aluminum Alloy 6061T6 with Electroless nickel undercoat for attaining good EMI/EMC, Corrosion Protection & solderability for subsystem components of various satellites.

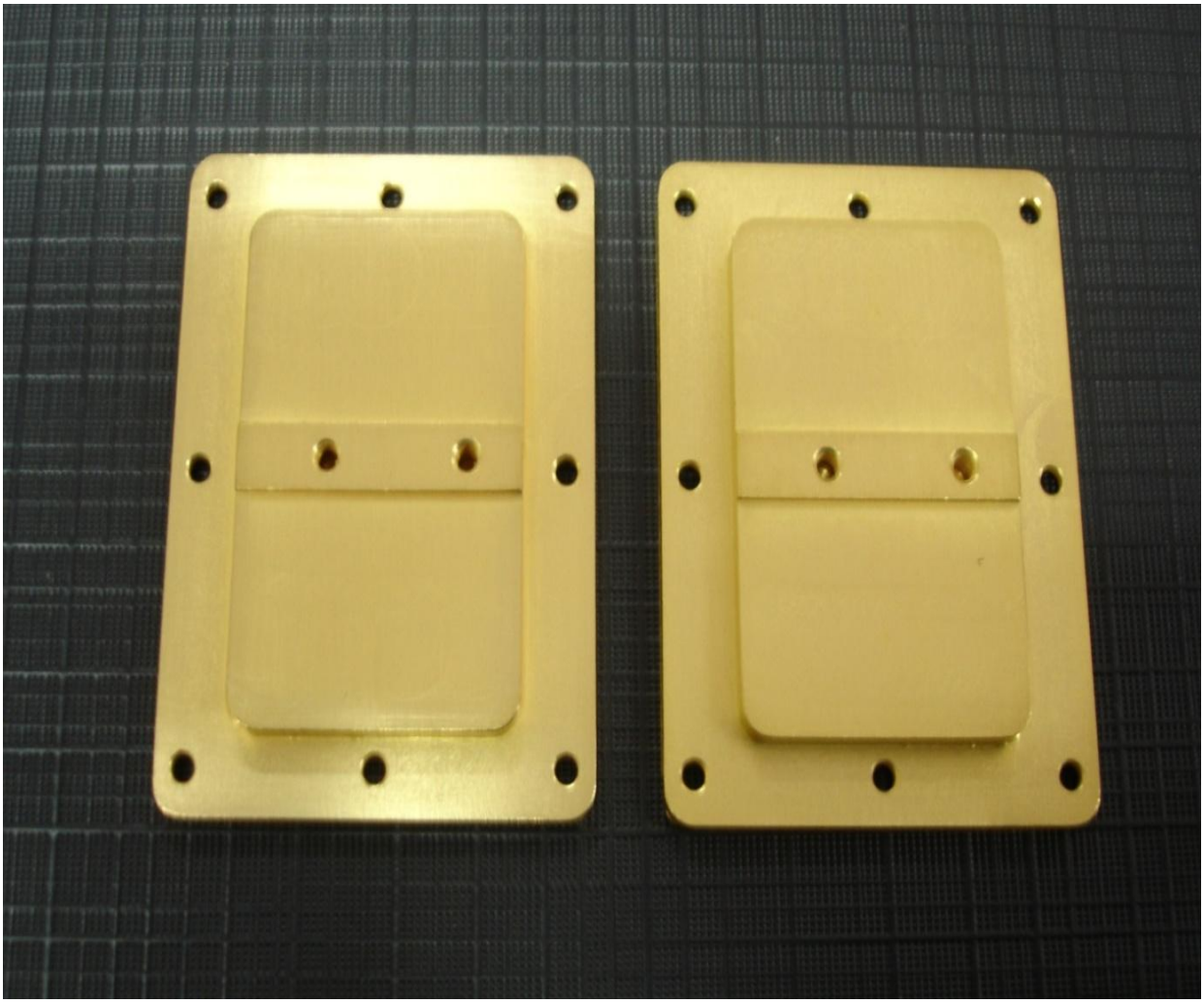
Technical Specifications		
Thickness of Electroless Nickel undercoat	8 -10µm	
Thickness of Gold plating	1µm	

77. Gold Plating on Aluminum 6061T6 Alloy	
Process UID No	**STPD / ST - 02**
Brief Description	Developed and qualified the process of Gold Plating on Aluminum Alloy 6061T6 with Electroless nickel undercoat for attaining good EMI/EMC, Corrosion Protection & solderability for subsystem components of various satellites.

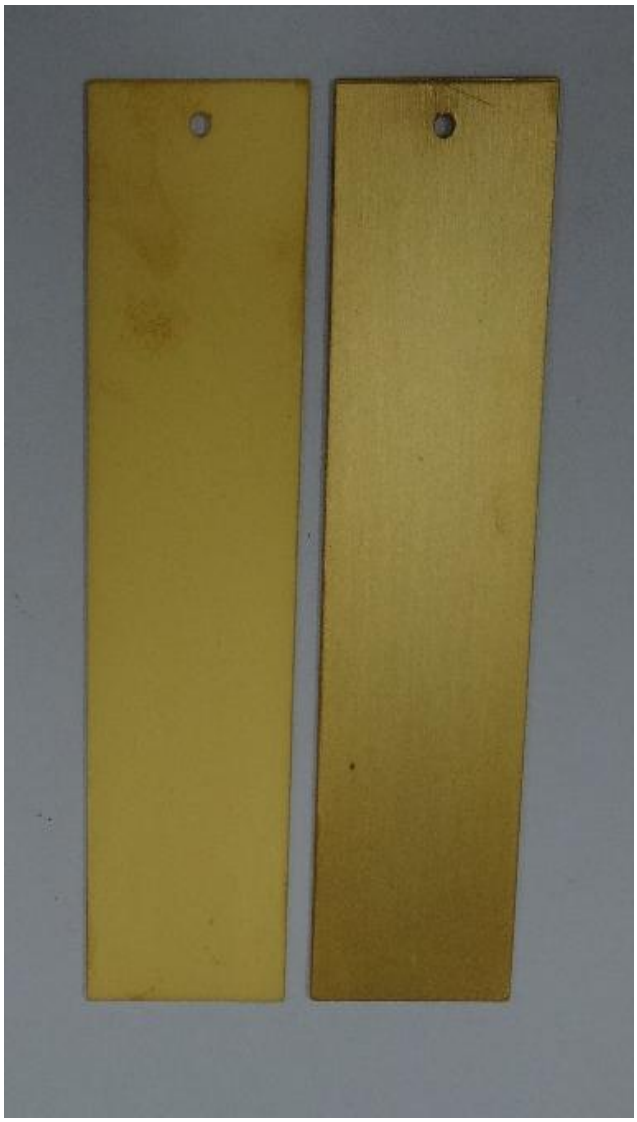


Technical Specifications	
Thickness of Electroless Nickel undercoat	8 -10µm
Thickness of Gold plating	2µm

78. Gold Plating on Kovar with Nickel Undercoat	
Process UID No	**STPD / ST – 03**
Brief Description	Developed and qualified the process of Gold Plating on Kovar with Nickel undercoat for attachment of gold plated Alumina substrates to carrier plates.



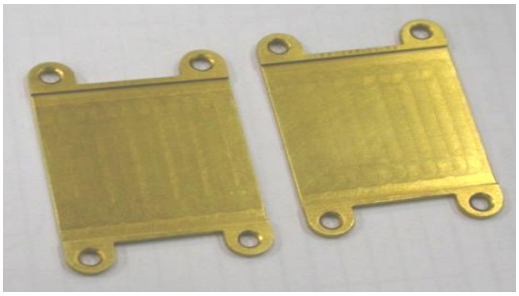
Technical Specifications	
Thickness of Nickel undercoat	3 - 4µm
Thickness of Gold plating	1.25 – 1.5µm

79. Gold Plating on Invar	
Process UID No	**STPD / ST – 04**
Brief Description	Developed and qualified the process of Gold Plating on Invar for solderability and corrosion protection for Induction posts.
	
Technical Specifications	
Thickness of Gold plating: 6µm	

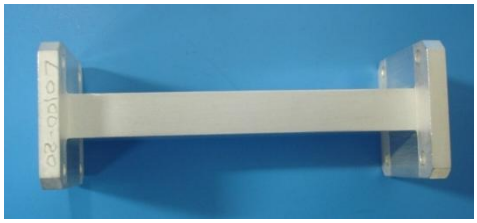
80. Gold Plating on SS-304	
Process UID No	**STPD / ST - 05**
Brief Description	Developed and qualified the process of Gold Plating on SS-304 for attaining good Electrical conductivity and good corrosion protection for SS-304 screws used in satellites.

Technical Specifications	
Thickness of Gold plating	6µm

81. Gold Plating on Magnesium AZ31B Alloy	
Process UID No	**STPD / ST - 06**
Brief Description	Developed and qualified the process of Gold Plating on Magnesium AZ31B alloy on PCPU boxes for attaining Corrosion Protection, good EMI/EMC & solderability.
	
Technical Specifications	
Thickness of Gold plating	6µm

82. Gold Plating on Silvar	
Process UID No	**STPD / ST - 07**
Brief Description	Developed and qualified the process of Gold Plating on Silvar (which provides an improved thermal conductivity along with a CTE that matches that of alumina substrate).
	
Technical Specifications	
Thickness of Nickel undercoat	3 - 4 µm
Thickness of Gold plating	1.5 – 2.5 µm

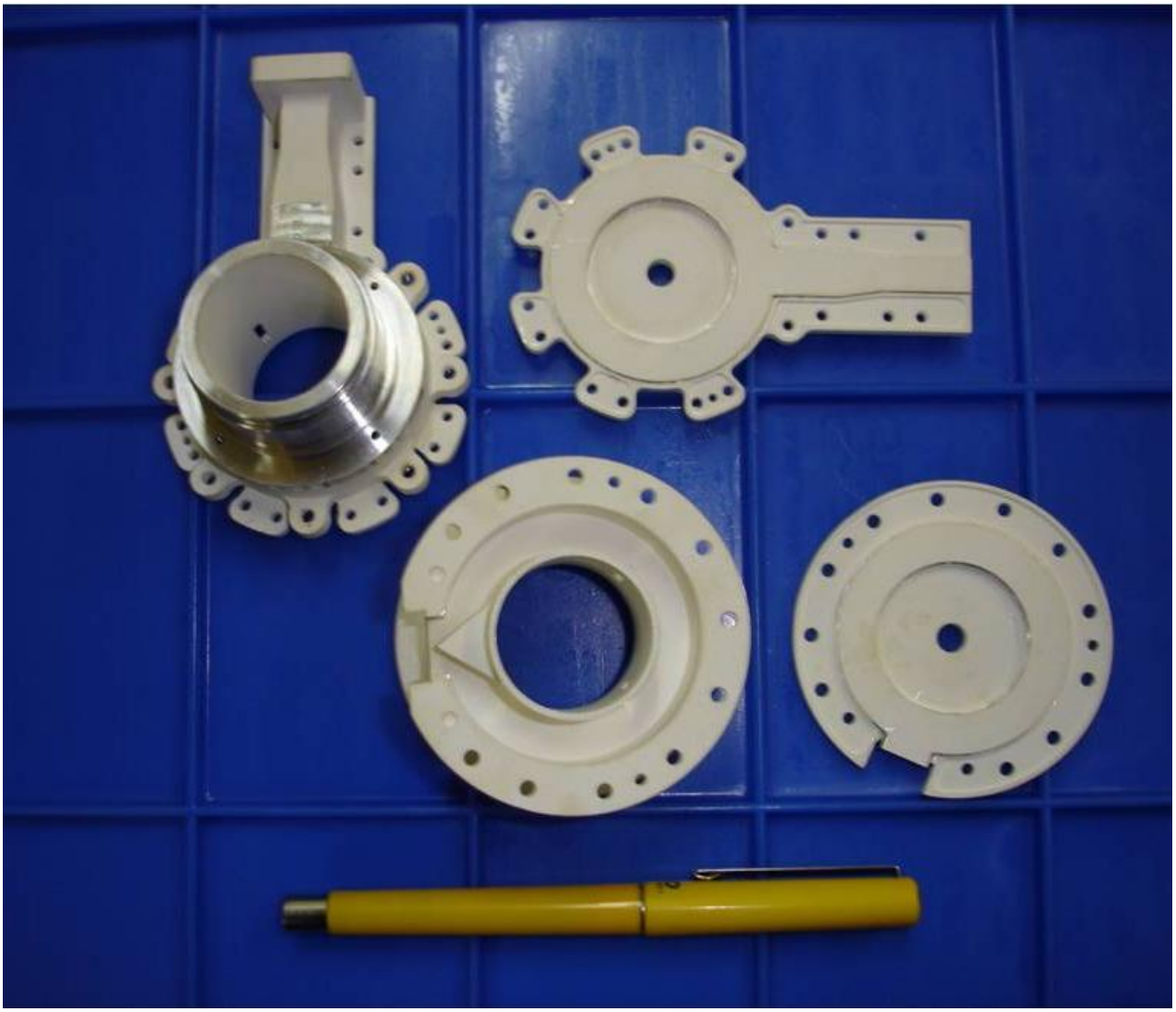
83. Gold Plating on CE-7	
Process UID No	**STPD / ST – 08**
Brief Description	Developed and qualified the process of Gold Plating on CE-7, which has low CTE.
	
Technical Specifications	
Thickness of Electroless Nickel	11-12 µm
Thickness of Gold plating	2 - 3 µm

84. Silver Plating on Aluminum 6061-T6 Alloy	
Process UID No	**STPD / ST – 09**
Brief Description	Developed and qualified the process of Silver Plating on Aluminum 6061-T6 Alloy on various components (Ku and Ka band) like waveguides, adaptors, HRFs, Filters for electrical conductivity & solderability, corrosion protection and good base for thermal control coatings.
	
Technical Specifications	
Thickness of Silver	5 - 8µm

85. 25-30 µm Silver Plating on Aluminum 6061-T6 Alloy	
Process UID No	**STPD / ST – 10**
Brief Description	Developed and qualified the process of Silver Plating on Aluminum 6061-T6 Alloy on various components like UHF, Filters for electrical conductivity & solderability, corrosion protection and good base for thermal control coatings.

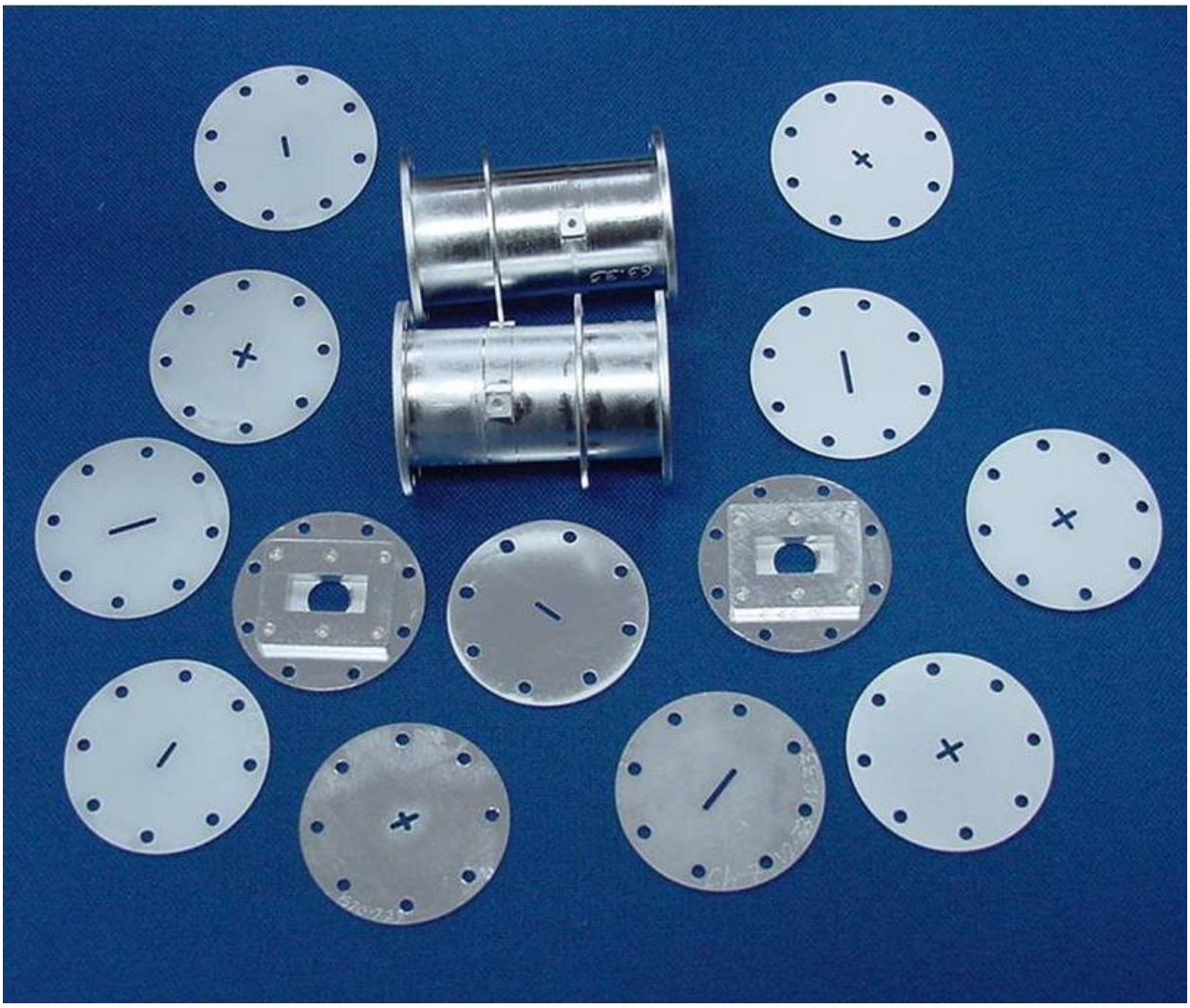
Technical Specifications	
Thickness of Silver	25 - 30µm

86. Silver Plating on Aluminum 2024 Alloy	
Process UID No	**STPD / ST - 11**
Brief Description	Developed and qualified the process of Silver Plating on Aluminum 2024 Alloy on various components like rotary joints for good electrical conductivity & solderability, corrosion protection and good base for thermal control coatings.



Technical Specifications	
Thickness of Silver	5 - 8µm

87. Silver Plating on Invar	
Process UID No	**STPD / ST - 12**
Brief Description	Developed and qualified the process of Silver Plating on Invar manifolds, cavities, iris, adaptors for good electrical conductivity & solderability and good base for thermal control coatings.



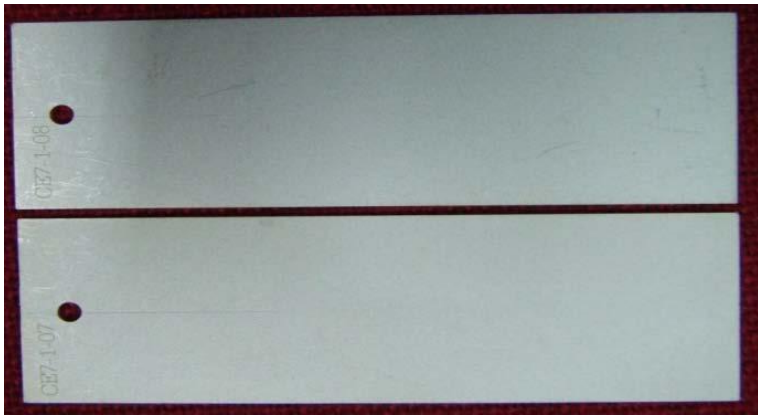
Technical Specifications	
Thickness of Silver	5 - 8µm

88. Silver Plating on Copper Helix

Process UID No	**STPD / ST – 13**
Brief Description	Developed and qualified the process of Silver Plating on copper helix conductors for solderability to helix and feed network.

Technical Specifications	
Thickness of Silver	5 - 8µm

89. Silver Plating on CE-7	
Process UID No	**STPD / ST – 14**
Brief Description	Developed and qualified the process of Silver Plating on CE-7, which has low CTE.



Technical Specifications	
Thickness of Electroless Nickel	10-12µm
Thickness of Silver	8-9µm

90. Silver Plating on Copper-Beryllium	
Process UID No	**STPD / ST – 15**
Brief Description	Developed and qualified the process of Silver Plating on Copper-Beryllium alloy with nickel undercoat for use as shims between waveguides.

Technical Specifications	
Thickness of Silver	4-7µm

91. Electroless Silver Plating on Aluminum 6061T6

Process UID No	**STPD / ST – 16**
Brief Description	Developed and qualified Electroless silver plating on Aluminum without passing electrolytic current between anode and cathode. This solves the problem of plating silver inside difficult to approach cavities like small cross sectional waveguides and similar components.

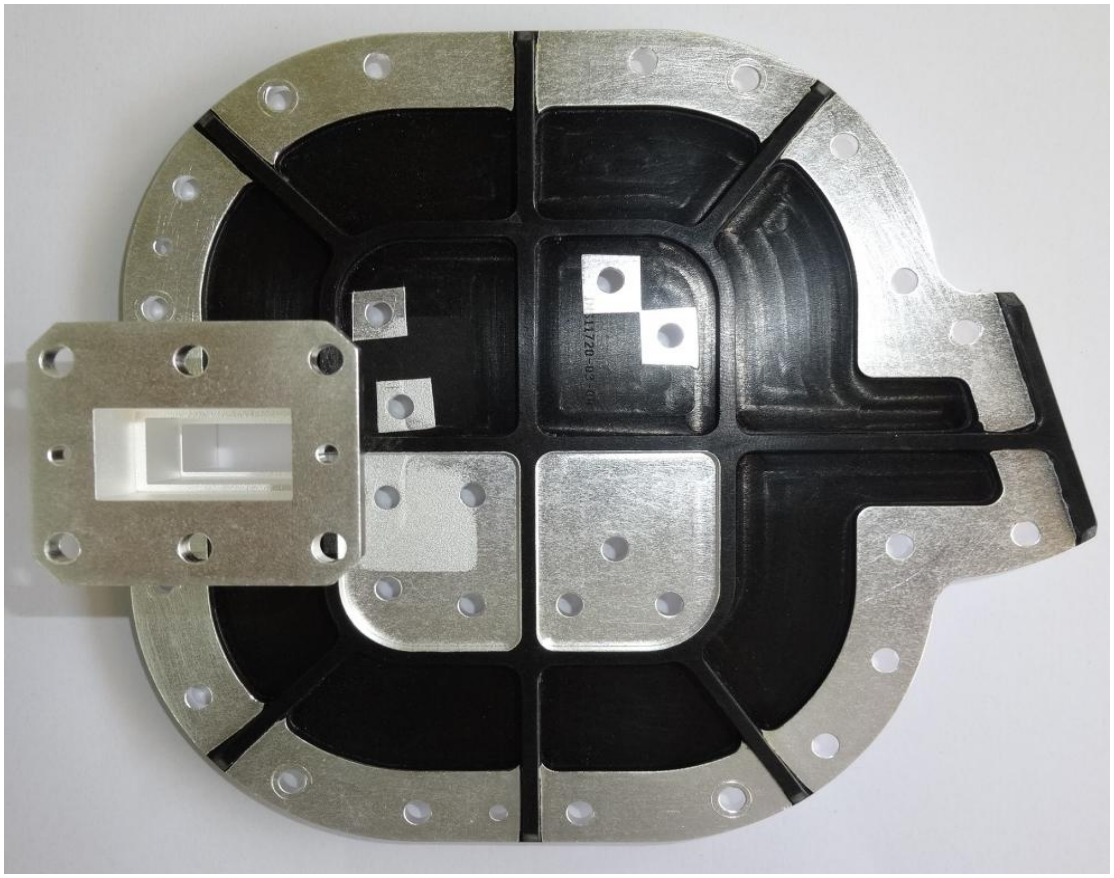
Technical Specifications	
Thickness of Electroless Nickel	8 - 12 µm
Thickness of Silver	2µm

92. Silver Plating on Kovar Pedestals

Process UID No	**STPD / ST – 17**
Brief Description	Developed and qualified the process of Silver Plating on Kovar pedestals as a product qualification to use in GSAT-11 Ku-band 116 MHz DR filters.

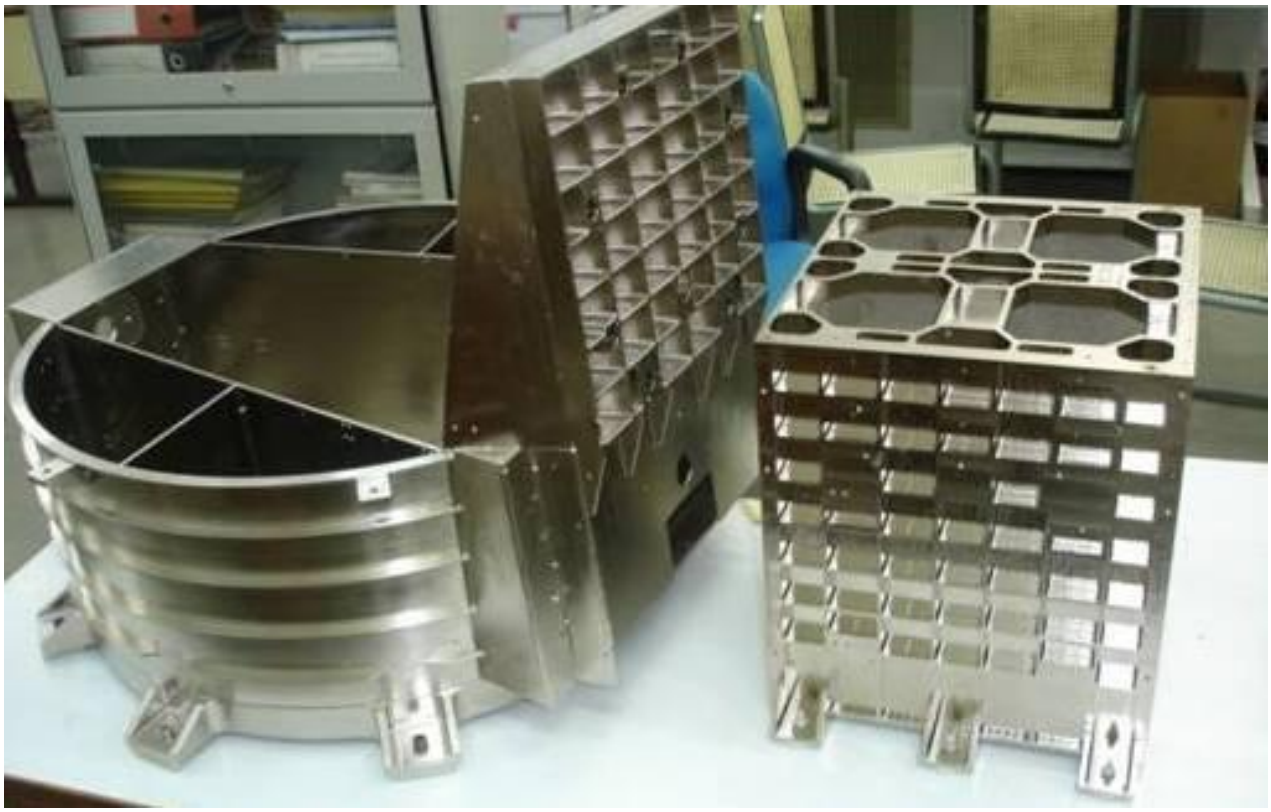
Technical Specifications	
Thickness of Nickel undercoat	3 - 4µm
Thickness of Silver	5 - 8µm

93. Black Anodizing and Silver Plating on 6061-T6 Aluminum Alloy	
Process UID No	**STPD / ST-18**
Brief Description	Developed and qualified the process of Black Anodizing and Silver Plating on Aluminum 6061-T6 Alloy for getting good electrical conductivity, solderability inside and high emissivity and high Absorptivity outside various filters and adapters.



Technical Specifications	
Thickness of Silver	4-10µm
Thickness of Black Anodizing	22-25µm
Emissivity (ε)	0.9 ± 0.02
Solar Absorptivity (α)	> 0.91

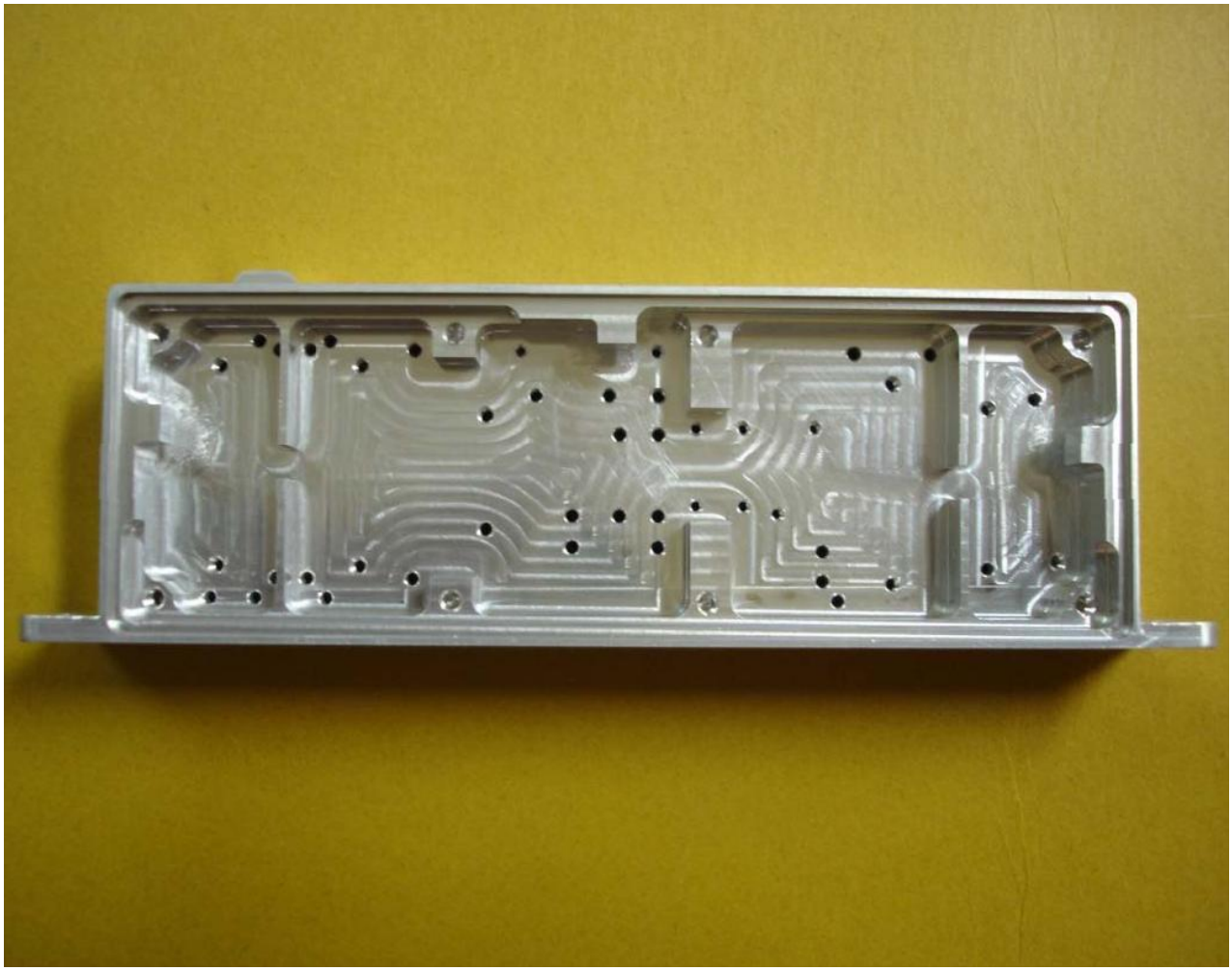
94. Electroless Nickel Plating on Invar	
Process UID No	**STPD / ST-19**
Brief Description	Developed and qualified the process of Electroless Nickel Plating on Invar Optical structures, mirror mounts etc., for corrosion protection and good base for thermal control coatings.



Technical Specifications	
Thickness of Electroless Nickel Plating	8 - 12µm

95. Electroless Nickel Plating on Aluminum 6061-T6 Alloy

Process UID No	**STPD / ST-20**
Brief Description	Developed and qualified the process of Electroless Nickel Plating on Aluminum boxes and covers for getting corrosion protection and good base for thermal control coatings.



Technical Specifications

Thickness of Electroless Nickel Plating	8 - 12µm

96. Anodizing on Aluminum 6061-T6 Alloy	
Process UID No	**STPD / ST-21**
Brief Description	Developed and qualified the process of Anodizing on Aluminum 6061-T6 Alloy for getting nonconductive surface, corrosion protection, and good base for Thermal Control coatings.

Technical Specifications

Thickness of Anodizing	10 ± 2µm

97. Black Anodizing on Aluminum 6061-T6 Alloy	
Process UID No	**STPD / ST-22**
Brief Description	Developed and qualified the process of Black Anodizing on Aluminum 6061-T6 Alloy packages to achieve high emissivity & solar absorptivity, nonconductive surface, corrosion protection.

Technical Specifications	
Thickness of Black Anodizing	25-28µ
Emissivity (ε)	0.9 ± 0.02
Solar Absorptivity (α)	> 0.91

98. Black Anodizing by Immersion Process on Aluminum 6061-T6 Alloy	
Process UID No	**STPD / ST-23**
Brief Description	Developed and qualified an alternative process for black anodizing on Aluminum 6061T6 alloy (to electrolytic black anodizing) which is a 2 solution dip - immersion process.

Technical Specifications	
Thickness of Black Anodizing	25µm
Emissivity (ε)	0.89 – 0.90
Solar Absorptivity (α)	> 0.88

99. Chromate conversion coating on Aluminum 6061T6 Alloy	
Process UID No	**STPD / ST-24**
Brief Description	Developed and qualified the process of Chromate conversion coating on Aluminum 6061T6 alloy for corrosion protection, electrical conductivity and good base for thermal control coatings.

Technical Specifications	
Thickness of Chromate Surface	1µm

100. Chromating & Black Anodizing on Aluminum 6061T6 Alloy	
Process UID No	**STPD / ST-25**
Brief Description	Developed and qualified the process of Black anodizing and Chromating on Aluminum 6061T6 alloy packages. Black anodizing to achieve high emissivity & solar absorptivity, electrical insulating surface and corrosion protection and Chromating to retain electrical conductivity, corrosion protection and good base for thermal control coatings.

Technical Specifications	
Thickness of Chromating	1µm
Thickness of Black Anodizing	25 - 28µm
Emissivity (ε)	0.9 ± 0.02
Solar Absorptivity (α)	≥ 0.91

101. Chromate conversion coating on Magnesium AZ31B Alloy	
Process UID No	**STPD / ST-26**
Brief Description	Developed and qualified the process of Chromate conversion coating on Magnesium AZ31B Alloy for corrosion protection, electrical conductivity and good base for thermal control coatings.

Technical Specifications	
Thickness of chromate surface	1µ

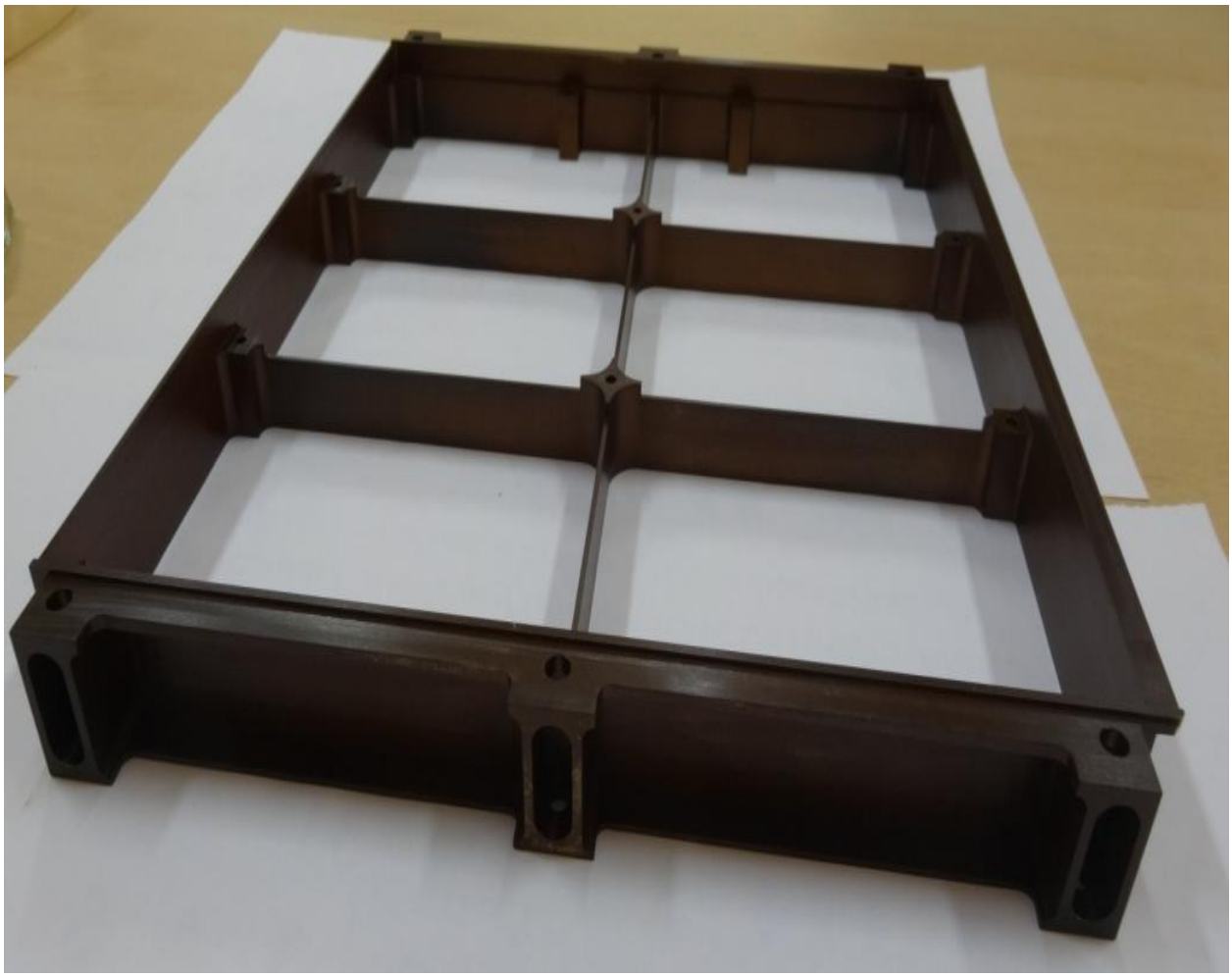
102. Black Anodizing on Magnesium Alloy AZ-31B

Process UID No	**STPD / ST – 27**
Brief Description	Developed and qualified the process of Black Anodizing on Magnesium Alloy AZ31B Alloy packages to achieve high emissivity & solar absorptivity, nonconductive surface, corrosion protection.

Technical Specifications

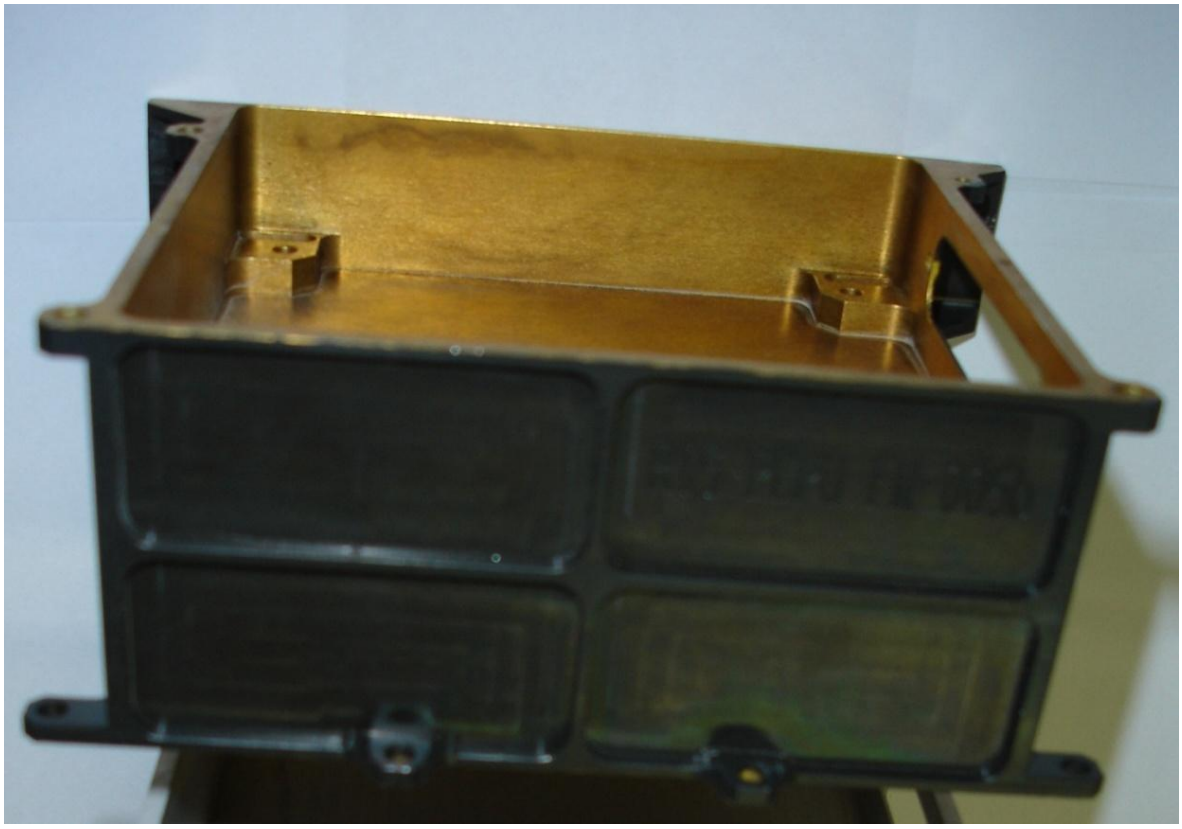
Thickness of Black Anodizing	4-7µm
Emissivity (ε)	0.75 ± 0.05
Solar Absorptivity (α)	0.8

103. Galvanic Anodizing on Magnesium Alloy AZ-31B	
Process UID No	**STPD / ST – 28**
Brief Description	Developed and qualified the process of Galvanic Anodizing on Magnesium Alloy AZ31B Alloy packages to achieve high emissivity & solar absorptivity, nonconductive surface, corrosion protection.



Technical Specifications	
Thickness of Black Anodizing	3-5µm
Emissivity (ε)	0.72 – 0.79
Solar Absorptivity (α)	0.83 – 0.88

104. Black Anodizing and Chromate conversion coating on Magnesium Alloy AZ-31B	
Process UID No	**STPD / ST- 29**
Brief Description	Developed and qualified the process of Black Anodizing and Chromate conversion coating on Magnesium Alloy AZ-31B, for getting nonconductive surface, Optical properties like emissivity and absorptivity, corrosion resistance and good base for paint for subsystem components of various satellites.



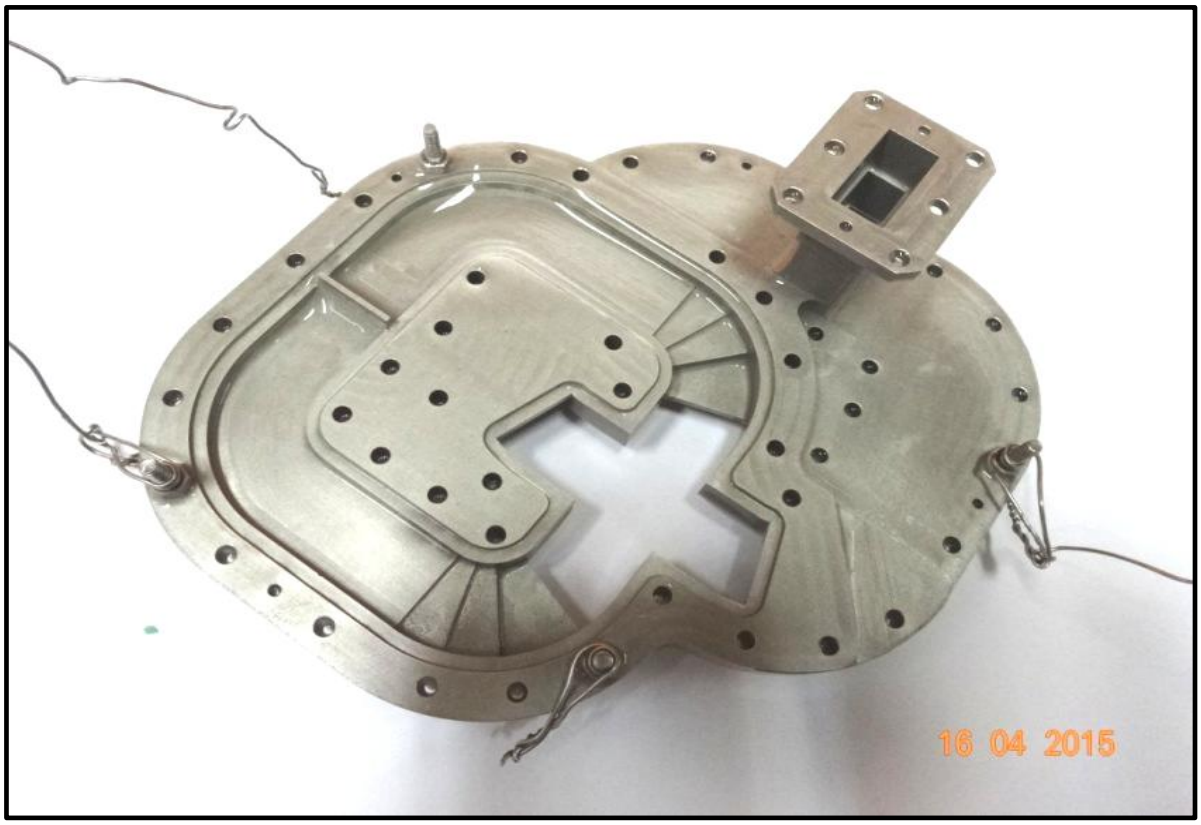
Technical Specifications	
Thickness of Black Anodizing	4-7µm
Emissivity (ε)	0.75 ± 0.05
Solar Absorptivity (α)	0.8
Thickness of chromate surface	1-2µm

105. Black Nickel Plating on Invar

Process UID No	**STPD / ST- 30**
Brief Description	Developed and qualified the process of Black Nickel on Invar to achieve optical properties suitable for electro-optical payloads.

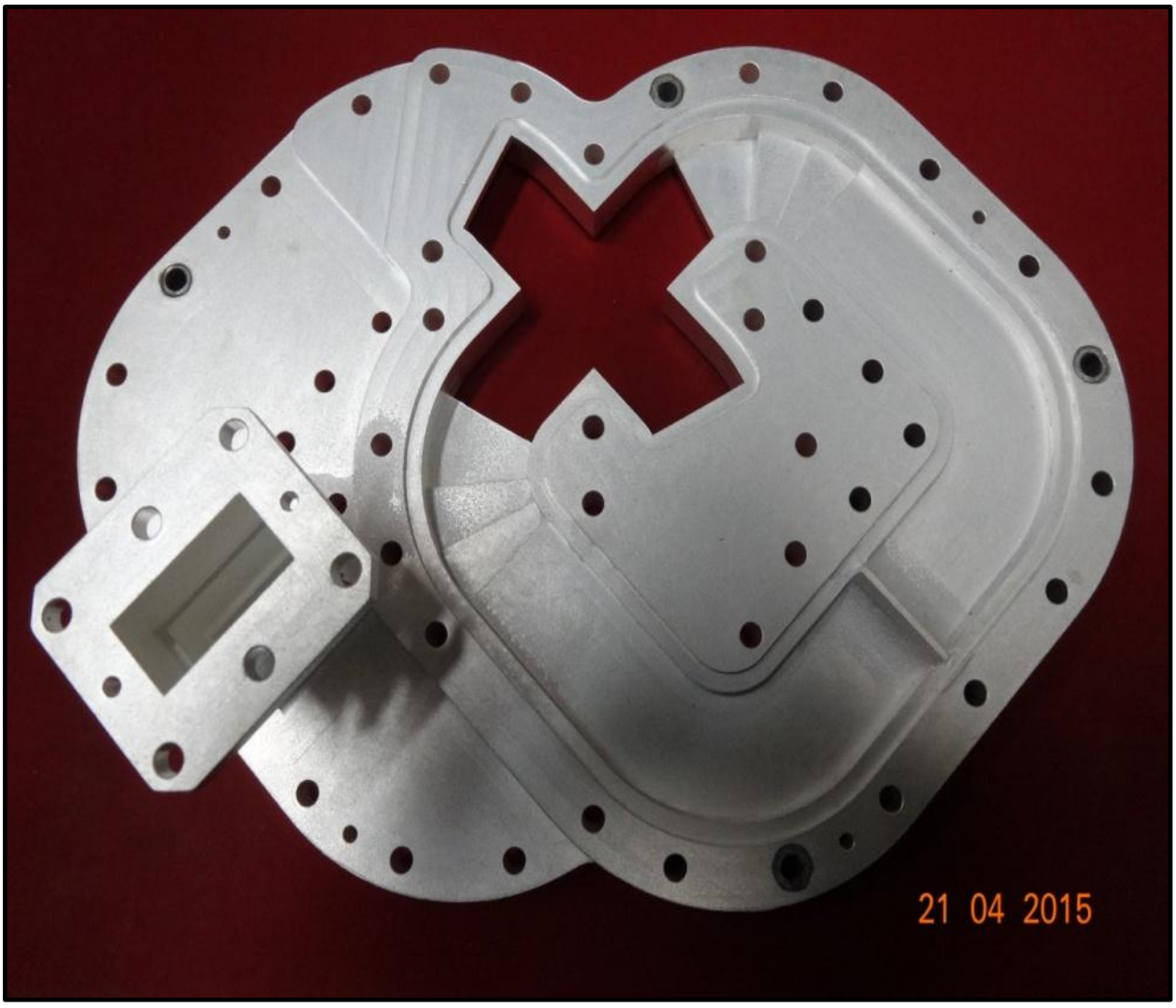
Technical Specifications	
Thickness of Black Nickel Plating	10 - 15 µm
Emissivity (ε)	≥0.71
Solar Absorptivity (α)	≥0.90

106. Electroless Nickel Plating on Magnesium AZ31B Alloy	
Process UID No	**STPD / ST- 31**
Brief Description	Developed and qualified the process of Electroless nickel plating on Magnesium AZ31B alloy boxes and covers for corrosion resistance and good base for thermal control coatings.



Technical Specifications	
Thickness of Black Nickel Plating	8 - 12 µm

107. Silver Plating on Magnesium AZ31B Alloy	
Process UID No	**STPD / ST- 32**
Brief Description	Developed and qualified the process of Silver plating on Magnesium AZ31B Alloy components like UHF, OMT cavity, filters for electrical conductivity & solderability, corrosion resistance and good base for thermal control coatings.



Technical Specifications	
Thickness of Silver Plating	4 - 6 µm

108. Fluoride Treatment on Magnesium AZ31B Alloy

Process UID No	**STPD / ST- 33**
Brief Description	Developed and qualified the processs of Fluoride treatment on Magnesium AZ31B Alloy packages to achieve high emmisivity & solar absorptivity, non conductive surface, corrosion protection, and good base for thermal control coatings.

Technical Specifications

Thickness of Black Nickel Plating	4 - 6 µm
Emissivity (ε)	≥0.75
Solar Absorptivity (α)	≥0.90
Salt Spray Resistance	≥ 24 Hrs

109. Black Nickel Plating on Magnesium AZ31B Alloy

Process UID No	**STPD / ST- 34**
Brief Description	Developed and qualified the processs of Black nickel plating on Magnesium packages and covers for getting good electrical conductivity, solderability, optical properties, corrosion protection and good base for thermal control coatings.

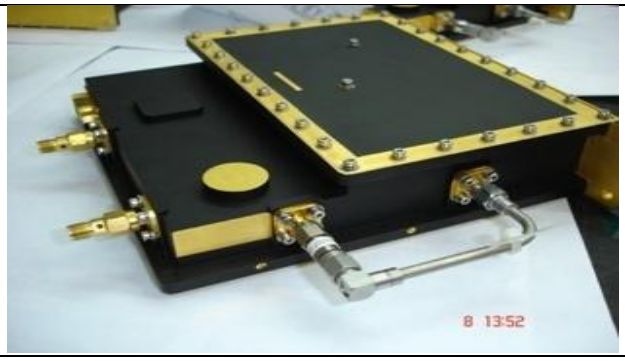
Technical Specifications

Thickness of Black Nickel Plating	18 - 20 µm
Emissivity (ε)	≥0.85
Solar Absorptivity (α)	≥0.92
Salt Spray Resistance	≥ 24 Hrs

110. Black Thermal Control Coating for High Emissivity & Solar Absorptivity

Process UID No	**STPD / TP - 01**
Brief Description	Developed and qualified the process of Black Thermal Control coating with high emissivity and solar absorptivity to facilitate radiant heat transfer among internal components of satellites. This process is qualified on following different base substrates:-

➢ Anodized Aluminum 6061T6 alloy ➢ Chromated Aluminum 6061T6 alloy ➢ Aluminum 6061T6 alloy ➢ Electroless Nickel Plated Al 6061T6 ➢ Silver plated Aluminum 6061T6 alloy ➢ Gold plated Aluminum 6061T6 alloy ➢ Aluminum 2024 alloy	➢ Silver plated Aluminum 2024 alloy ➢ Invar ➢ Electroless Nickel plated Invar ➢ Silver plated Invar ➢ Magnesium AZ31B alloy ➢ Black Anodized Magnesium AZ31B alloy ➢ Chromated Magnesium AZ31B alloy



Technical Specifications

Dry Film Thickness	50-75 µm
Appearance &Colour	Flat Black
Emissivity (ε)	>0.90
Solar Absorptivity (α)	> 0.94
Surface Resistance	≥ 10^{10} ohm/square
Total Mass Loss (TML)	≤ 1.00%
Collected Volatile Condensable Material (CVCM)	≤ 0.10%
Curing Time to Use	≥ 7 days
Vacuum Baking for Optical Components	65 °C/24 hours/10^{-5} torr (or) 50 °C/48hours/10^{-5} torr

111. Black Thermal Control Coating for High Temperature Applications

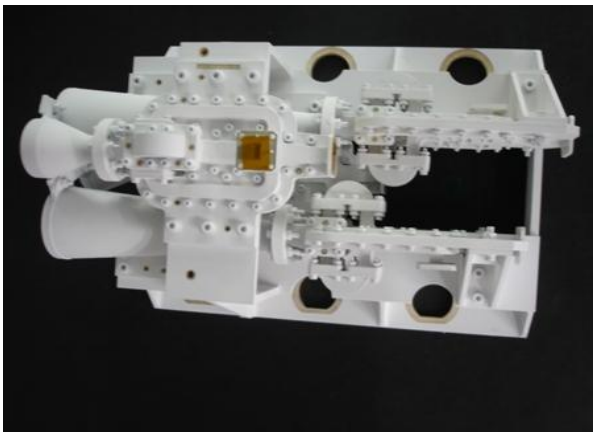
Process UID No	**STPD / TP - 02**
Brief Description	Developed and qualified the process of Black Thermal Control coating for High Temperature applications with high emissivity and solar absorptivity to facilitate radiant heat transfer. This process is qualified on Anodized Aluminum 6061T6 alloy.

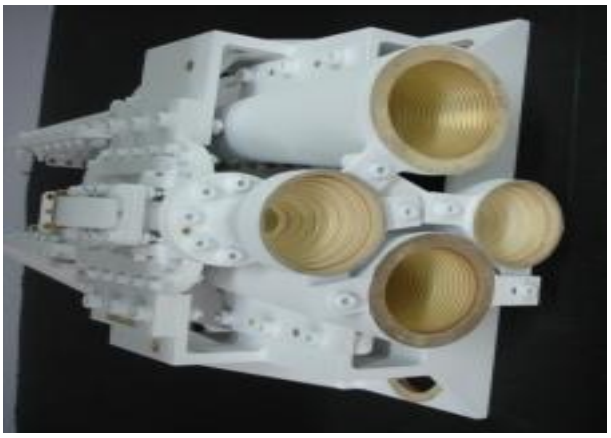
Technical Specifications

Dry Film Thickness	80-110 µ
Appearance &Colour	Matt Black
Emissivity (ε)	≥ 0.90
Solar Absorptivity (α)	≥ 0.94
Temperature Range	up to 250 °C
Surface Resistance	≥ 10^{10} ohm/square
Total Mass Loss (TML)	≤ 1.00%
Collected Volatile Condensable Material (CVCM)	≤ 0.10%
Curing Time to Use	7 days
Vacuum Baking for Optical Components	65 °C/24 hours/10^{-5} torr (or) 50 °C/48hours/10^{-5} torr

112. White Thermal Control Coating for High Temperature Applications

Process UID No	**STPD / TP - 03**
Brief Description	Developed and qualified the process of White Thermal Control coating for high temperature applications with high emissivity and high reflectivity for components exposed to direct solar radiation. This process is qualified on Silver plated Aluminum Alloy 6061T6 alloy.



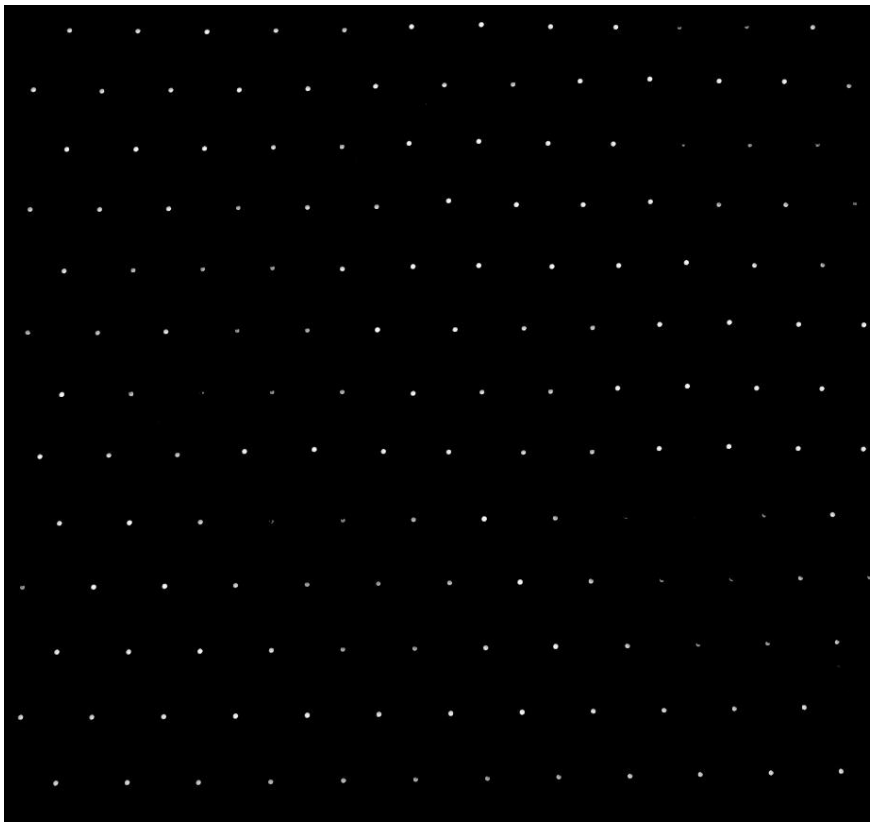


Technical Specifications

Dry Film Thickness	100-130 µm
Appearance & Colour	Flat White
Emissivity (ε)	≥ 0.88
Solar Absorptivity (α)	≥ 0.20
Temperature Range	Up to 250 °C
Surface Resistance	≥ 10^{10} ohm/square
Total Mass Loss (TML)	≤ 1.00%
Collected Volatile Condensable Material (CVCM)	≤ 0.10%
Curing Time to Use	7 days
Vacuum Baking for Optical Components	65 °C / 24 hours / 10^{-5} torr (or) 50 °C / 48hours / 10^{-5} torr

113. Black Thermal Control Coating on Kapton Tape

Process UID No.	**STPD / TP - 04**
Brief Description	Developed and qualified the process of Black Thermal Control coating on Kapton Tape with adhesive transfer sheet.



Technical Specifications

Dry Film Thickness	35-50 µm
Appearance & Colour	Flat Black
Emissivity (ε)	>0.90
Solar Absorptivity (α)	> 0.94
Total Mass Loss (TML)	≤ 1.00%
Collected Volatile Condensable Material (CVCM)	≤ 0.10%
Curing Time to Use	7 days

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